



A960M-MV

Rev:1.0A

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REVISION HISTORY:

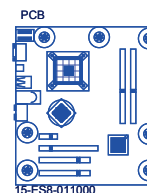
Rev	Date	Notes
1.0	2012-08-23	INITIAL RELEASE 1. Change SIO from F71869E to F71808A 2. Change DVI to HDMI
1.0A	2012-10-05	1. Swap HDMI signal

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example 1) DESIGN NOTES in text for the design note to grey are information show the note inside the notes.
colored box.

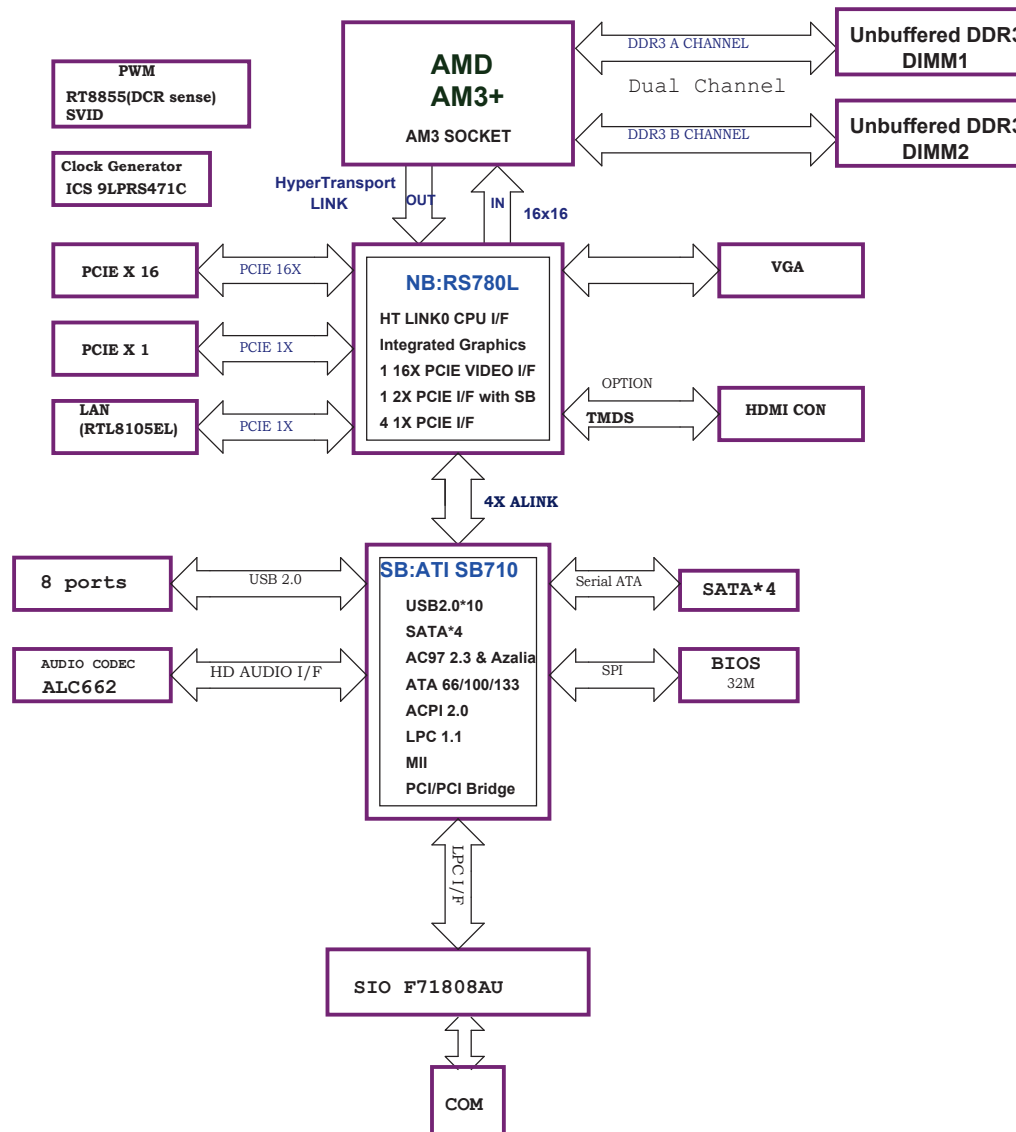
DESIGN NOTE: Example 2) DESIGN NOTES in text for the design note to yellow are notes of show the note inside the caution.
colored box.

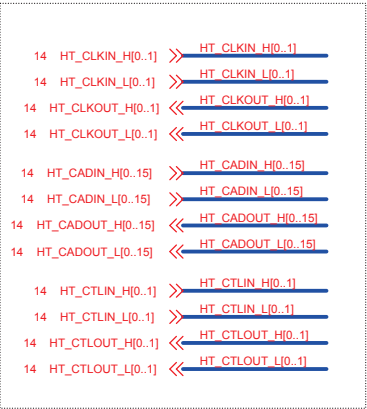
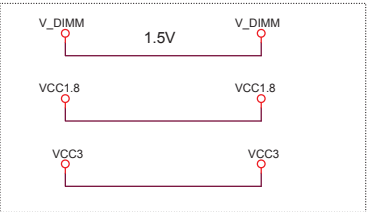
DESIGN NOTE: Example 3) DESIGN NOTES in text for the design note to red are critical, and show the note inside the must be understood and followed.
colored box.



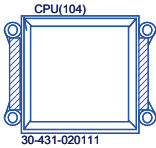
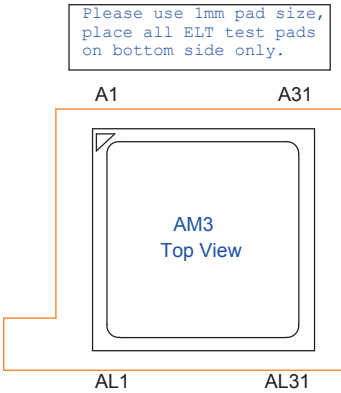
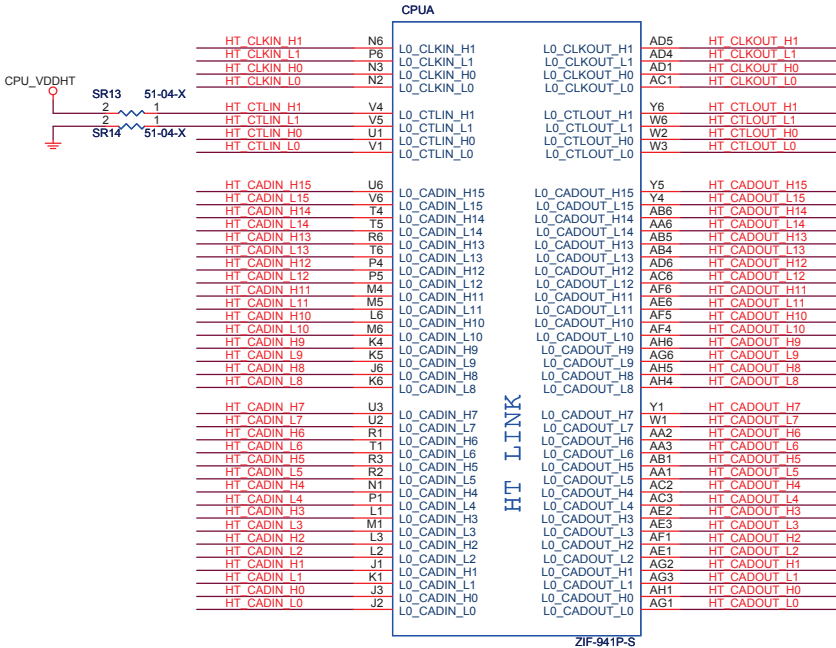
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

Elitegroup Computer Systems			
Title Cover Page			
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Date: Thursday, October 11, 2012		Sheet 1	of 32



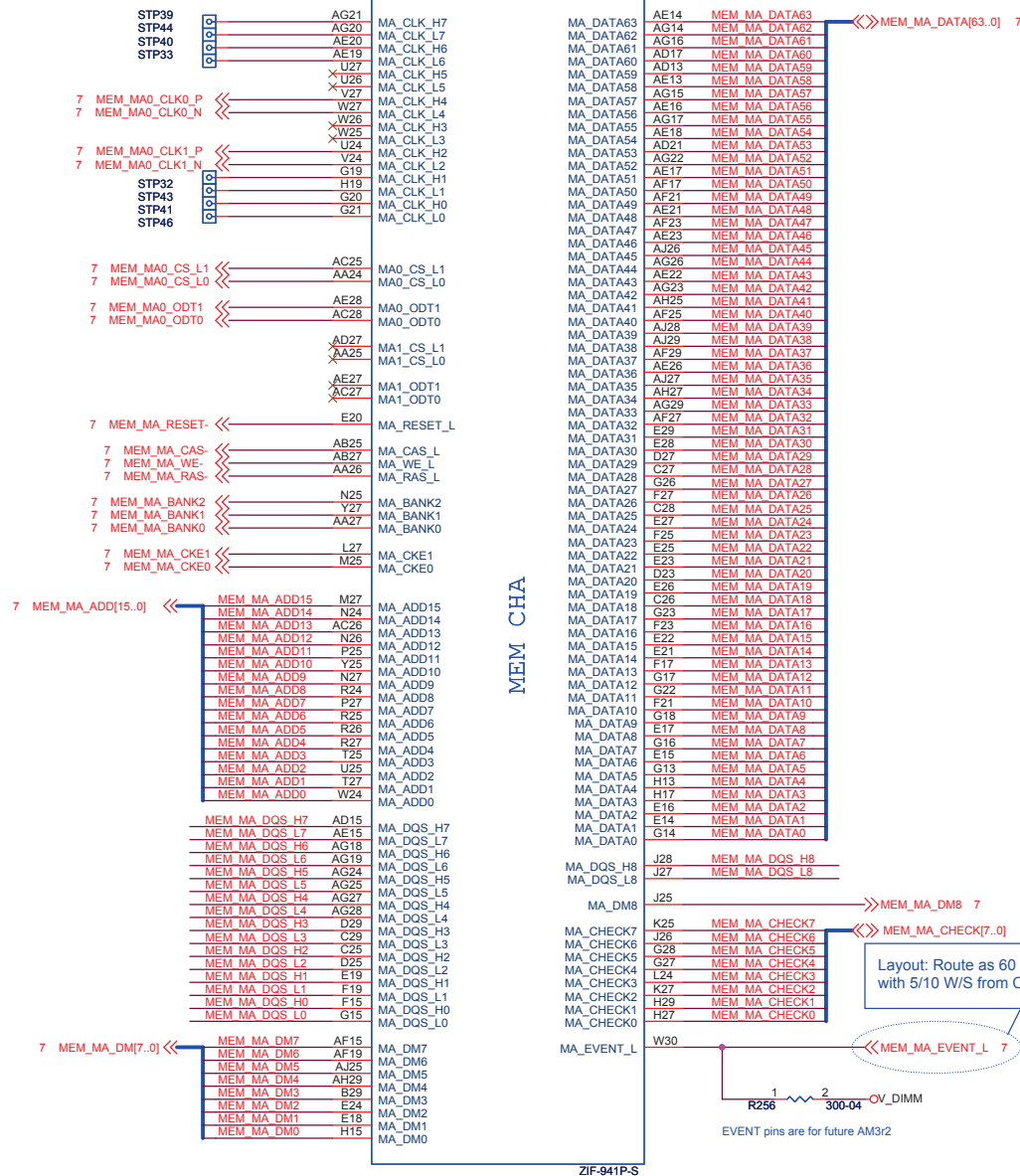


HyperTransport



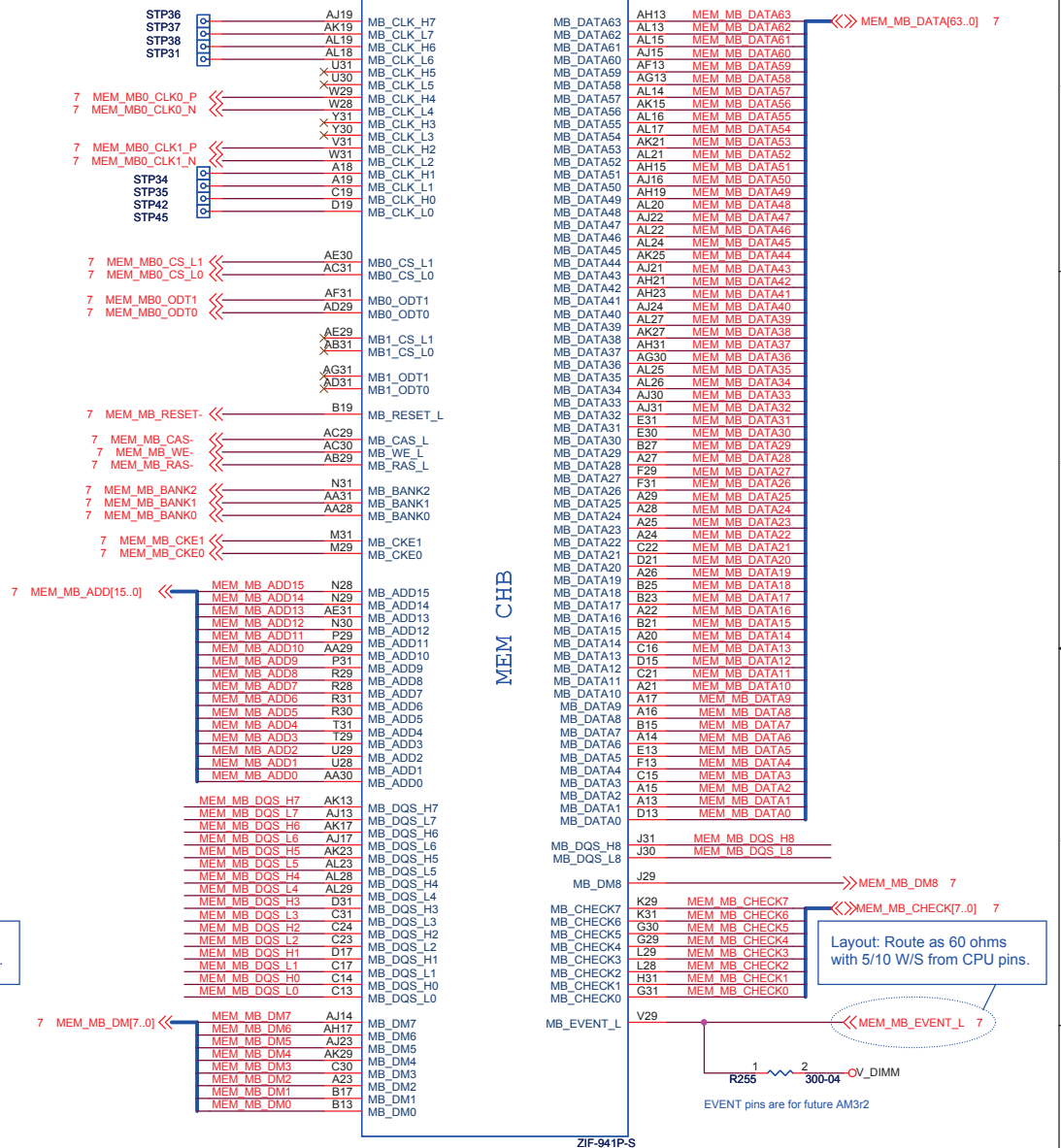
DDR3 Memory Interface A

CPUCB

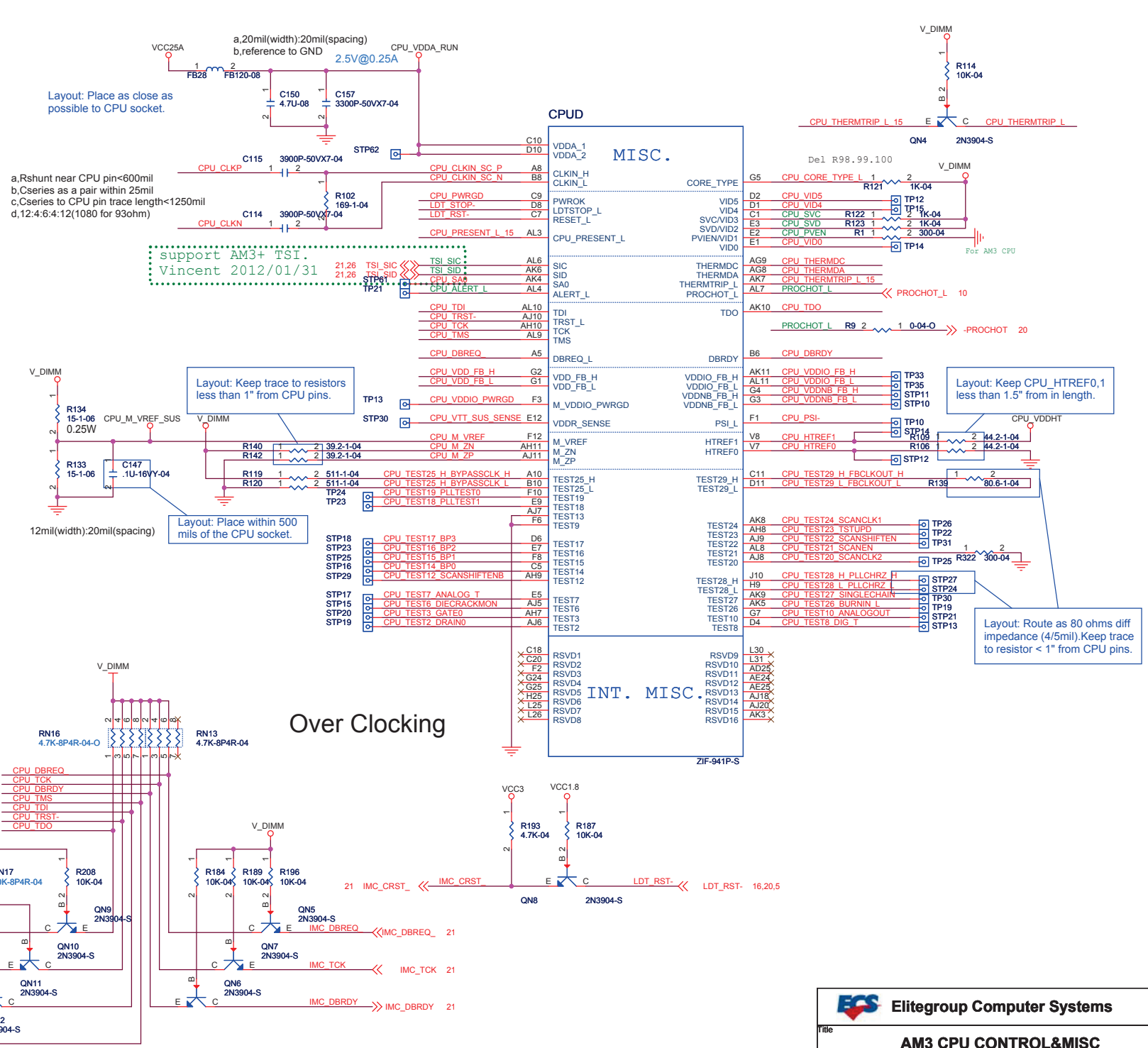
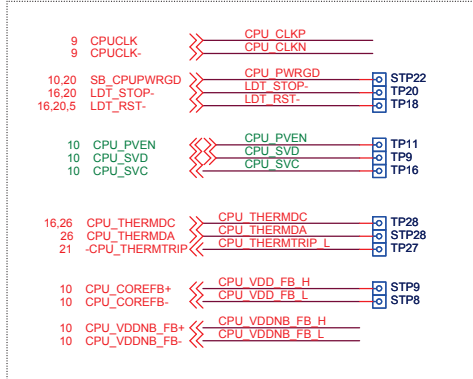


DDR3 Memory Interface B

CPUCB



CPU Memory



Processor Power and Ground

CPU

CPUH

CPUG

CPUVDD

POWER / GND1

POWER / GND2

POWER / GND3

POWER / GND4

POWER / GND5

POWER / GND6

POWER / GND7

POWER / GND8

POWER / GND9

POWER / GND10

POWER / GND11

POWER / GND12

POWER / GND13

POWER / GND14

POWER / GND15

POWER / GND16

POWER / GND17

POWER / GND18

POWER / GND19

POWER / GND20

POWER / GND21

POWER / GND22

POWER / GND23

POWER / GND24

POWER / GND25

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POWER / GND208

POWER / GND209

POWER / GND210

POWER / GND211

POWER / GND212

POWER / GND213

POWER / GND214

POWER / GND215

POWER / GND216

POWER / GND217

POWER / GND218

POWER / GND219

POWER / GND220

POWER / GND221

POWER / GND222

POWER / GND223

POWER / GND224

POWER / GND225

POWER / GND226

POWER / GND227

POWER / GND228

POWER / GND229

POWER / GND230

POWER / GND231

POWER / GND232

POWER / GND233

POWER / GND234

POWER / GND235

POWER / GND236

POWER / GND237

POWER / GND238

POWER / GND239

The schematic diagram illustrates the power distribution network for the CPU. It features two primary power rails: **V_DIMM** and **CPU_VDD_RUN**.

V_DIMM Rail: This rail is connected to a 1U-16VY-08X-O source. It includes several capacitors: SC74 (10U-10VY5-08X-O), SC71 (10U-10VY5-08X-O), SC68 (10U-6V3X5-08X-O), and SC76 (10U-25VX-04-X). The rail is also connected to a 1U-10VY5-04-X source.

CPU_VDD_RUN Rail: This rail is connected to a 1U-10VY5-08X-O source. It includes several capacitors: SC56 (10U-10VY5-08X-O), SC61 (10U-10VY5-08X-O), SC59 (10U-10VY5-08X-O), SC58 (22U-10VY5-04-X), SC55 (10U-6V3X5-08-X), SC63 (10U-6V3X5-08-X), SC48 (10U-10VY5-08X-O), SC52 (10U-10VY5-08X-O), SC64 (10U-10VY5-08X-O), SC49 (10U-10VY5-08X-O), and SC55 (10U-6V3X5-08-X). The rail is also connected to a 1U-25VX-04-X source.

A detailed inset shows the connection of capacitor C165 to a 1U-16VY-04 source, with a 1U-16VY-04 source and a 1U-16VY-04 source connected to the rail.

FOR EMC

VDDR_HT3

C165

1 2

.1U-16VY-04

CPU_VDD_RUN

SC41

1 2

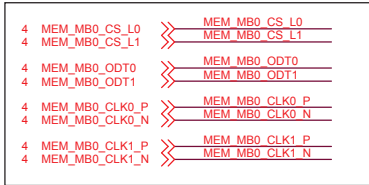
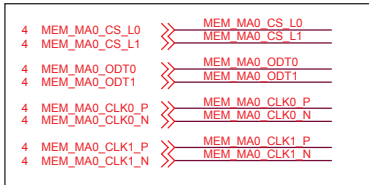
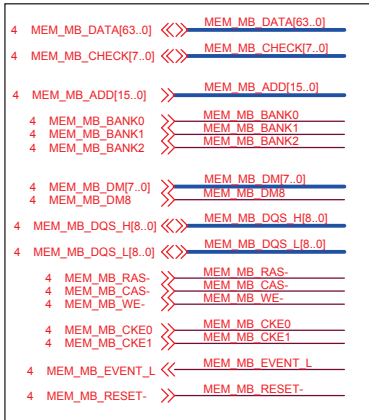
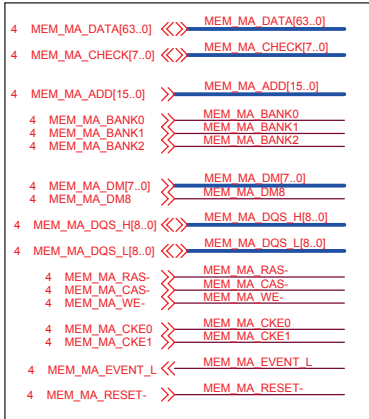
22U-10VY5-04-X-0

CPU_VDDNB

C22

1

.1U-16VY-04



MEM MA ADD0	188	A0
MEM MA ADD1	181	A1
MEM MA ADD2	61	A2
MEM MA ADD3	180	A3
MEM MA ADD4	59	A4
MEM MA ADD5	58	A5
MEM MA ADD6	178	A6
MEM MA ADD7	56	A7
MEM MA ADD8	177	A8
MEM MA ADD9	175	A9
MEM MA ADD10	70	A10
MEM MA ADD11	55	A11
MEM MA ADD12	174	A12
MEM MA ADD13	196	A13
MEM MA ADD14	172	A14
MEM MA ADD15	171	A15
MEM MA BANK0	71	BA0
MEM MA BANK1	190	BA1
MEM MA BANK2	52	BA2

MEM MA DM0	125	DM0/DQS9
MEM MA DM1	134	DM1/DQS10
MEM MA DM2	143	DM2/DQS11
MEM MA DM3	152	DM3/DQS12
MEM MA DM4	203	DM4/DQS13
MEM MA DM5	212	DM5/DQS14
MEM MA DM6	221	DM6/DQS15
MEM MA DM7	230	DM7/DQS16
MEM MA DM8	161	DM8/DQS17

MEM MA DQS L0	6	DQS0
MEM MA DQS H0	7	DQS0
MEM MA DQS L1	15	DQS1
MEM MA DQS H1	16	DQS1
MEM MA DQS L2	24	DQS2
MEM MA DQS H2	25	DQS2
MEM MA DQS L3	33	DQS3
MEM MA DQS H3	34	DQS3
MEM MA DQS L4	84	DQS4
MEM MA DQS H4	85	DQS4
MEM MA DQS L5	93	DQS5
MEM MA DQS H5	94	DQS5
MEM MA DQS L6	102	DQS6
MEM MA DQS H6	103	DQS6
MEM MA DQS L7	111	DQS7
MEM MA DQS H7	112	DQS7
MEM MA DQS L8	42	DQS8
MEM MA DQS H8	43	DQS8

MEM MA RAS-	192	RAS
MEM MA CAS-	74	CAS
MEM MA WE-	73	WE

MEM MA0 CS L0	193	S0
MEM MA0 CS L1	76	S1

MEM MA CKE0	50	CKE0
MEM MA CKE1	169	CKE1

MEM MA0 ODT0	195	ODT
MEM MA0 ODT1	77	RSVD/ODT1

MEM MA0 CLK0 P	184	CK0
MEM MA0 CLK0 N	185	CK0

MEM MA0 CLK1 P	63	CK1
MEM MA0 CLK1 N	64	CK1

SCLK0	118	SCL
SDATA0	238	SDA

VCC3	236	VDDSPD
------	-----	--------

MEM MA0 CS L0	167	TEST
MEM MA0 CS L1	167	TEST

MEM MA0 ODT0	48	FREE1
MEM MA0 ODT1	49	FREE2
MEM MA0 CLK0 P	187	FREE3
MEM MA0 CLK0 N	198	FREE4

MEM MA0 CLK1 P	168	RESET
MEM MA0 CLK1 N	53	ERR_OUT
MEM MA0 CLK1 P	68	PAR_IN
MEM MA0 CLK1 N	79	RSVD/SPD

MEM MA0 CS L0	126	DQS9
MEM MA0 CS L1	135	DQS10
MEM MA0 CS L2	144	DQS11
MEM MA0 CS L3	153	DQS12
MEM MA0 CS L4	204	DQS13
MEM MA0 CS L5	213	DQS14
MEM MA0 CS L6	222	DQS15
MEM MA0 CS L7	231	DQS16
MEM MA0 CS L8	162	DQS17

DDR3 1A	DDR3-240P-GY
A0	
A1	
A2	
A3	
A4	
A5	
A6	
A7	
A8	
A9	
A10	
A11	
A12	
A13	
A14	
A15	
BA0	
BA1	
BA2	
DM0/DQS9	
DM1/DQS10	
DM2/DQS11	
DM3/DQS12	
DM4/DQS13	
DM5/DQS14	
DM6/DQS15	
DM7/DQS16	
DM8/DQS17	
DQS0	
DQS0	
DQS1	
DQS1	
DQS2	
DQS2	
DQS3	
DQS3	
DQS4	
DQS4	
DQS5	
DQS5	
DQS6	
DQS6	
DQS7	
DQS7	
DQS8	
DQS8	
RAS	
CAS	
WE	
S0	
S1	
CKE0	
CKE1	
ODT	
RSVD/ODT1	
CK0	
CK0	
CK1	
CK1	
SA0	
SA1	
SCL	
SDA	
VDDSPD	
TEST	
FREE1	
FREE2	
FREE3	
FREE4	
RESET	
ERR_OUT	
PAR_IN	
RSVD/SPD	

		DDR3 2A	
MEM MB ADD0	188	A0	
MEM MB ADD1	181	A1	
MEM MB ADD2	61	A2	
MEM MB ADD3	180	A3	
MEM MB ADD4	59	A4	
MEM MB ADD5	58	A5	
MEM MB ADD6	178	A6	
MEM MB ADD7	56	A7	
MEM MB ADD8	177	A8	
MEM MB ADD9	175	A9	
MEM MB ADD10	70	A10	
MEM MB ADD11	55	A11	
MEM MB ADD12	174	A12	
MEM MB ADD13	196	A13	
MEM MB ADD14	172	A14	
MEM MB ADD15	171	A15	
MEM MB BANK0		71	BA0
MEM MB BANK1		190	BA1
MEM MB BANK2		52	BA2
MEM MB DM0	125	DM0/DQS9	
MEM MB DM1	134	DM1/DQS10	
MEM MB DM2	143	DM2/DQS11	
MEM MB DM3	152	DM3/DQS12	
MEM MB DM4	203	DM4/DQS13	
MEM MB DM5	212	DM5/DQS14	
MEM MB DM6	221	DM6/DQS15	
MEM MB DM7	230	DM7/DQS16	
MEM MB DM8	161	DM8/DQS17	
MEM MB DQS L0	6	DQS0	
MEM MB DQS H0	7	DQS0	
MEM MB DQS L1	15	DQS1	
MEM MB DQS H1	16	DQS1	
MEM MB DQS L2	24	DQS2	
MEM MB DQS H2	25	DQS2	
MEM MB DQS L3	33	DQS3	
MEM MB DQS H3	34	DQS3	
MEM MB DQS L4	84	DQS4	
MEM MB DQS H4	85	DQS4	
MEM MB DQS L5	93	DQS5	
MEM MB DQS H5	94	DQS5	
MEM MB DQS L6	102	DQS6	
MEM MB DQS H6	103	DQS6	
MEM MB DQS L7	111	DQS7	
MEM MB DQS H7	112	DQS7	
MEM MB DQS L8	42	DQS8	
MEM MB DQS H8	43	DQS8	
MEM MB RAS-	192	RAS	
MEM MB CAS-	74	CAS	
MEM MB WE-	73	WE	
MEM MB0 CS L0	193	S0	
MEM MB0 CS L1	76	S1	
MEM MB CKE0	50	CKE0	
MEM MB CKE1	169	CKE1	
MEM MB0 ODT0	195	ODT	
MEM MB0 ODT1	77	RSVD/ODT1	
MEM MB0 CLK0 P	184	CK0	
MEM MB0 CLK0 N	185	CK0	
MEM MB0 CLK1 P	63	CK1	
MEM MB0 CLK1 N	64	CK1	
VCC3	117	SA0	
	237	SA1	
SCLK0	118	SCL	
SDATA0	238	SDA	
VCC3	236	VDDSPD	
	167	TEST	
	48	FREE1	
	49	FREE2	
MEM MB EVENT L	187	FREE3	
	198	FREE4	
MEM MB RESET-	168	RESET	
	53	RRR_OUT	
	68	PAR_IN	
	79	RSVD/SPD	

DDR3 2A	DDR3-240P-GY		
A0		D00	3 MEM MB DATA0
A1		D01	4 MEM MB DATA1
A2		D02	9 MEM MB DATA2
A3		D03	10 MEM MB DATA3
A4		D04	122 MEM MB DATA4
A5		D05	123 MEM MB DATA5
A6		D06	128 MEM MB DATA6
A7		D07	129 MEM MB DATA7
A8			
A9		D08	12 MEM MB DATA8
A10		D09	13 MEM MB DATA9
A11		D10	18 MEM MB DATA10
A12		D11	19 MEM MB DATA11
A13		DQ12	131 MEM MB DATA12
A14		DQ13	132 MEM MB DATA13
A15		DQ14	137 MEM MB DATA14
		DQ15	138 MEM MB DATA15
BA0			
BA1		DQ16	21 MEM MB DATA16
BA2		DQ17	22 MEM MB DATA17
		DQ18	27 MEM MB DATA18
		DQ19	28 MEM MB DATA19
		DQ20	140 MEM MB DATA20
		DQ21	141 MEM MB DATA21
		DQ22	146 MEM MB DATA22
		DQ23	147 MEM MB DATA23
			30 MEM MB DATA24
		DQ24	31 MEM MB DATA25
		DQ25	36 MEM MB DATA26
		DQ26	37 MEM MB DATA27
		DQ27	149 MEM MB DATA28
		DQ28	150 MEM MB DATA29
		DQ29	155 MEM MB DATA30
		DQ30	156 MEM MB DATA31
		DQ31	
			81 MEM MB DATA32
		DQ32	82 MEM MB DATA33
		DQ33	87 MEM MB DATA34
		DQ34	88 MEM MB DATA35
		DQ35	200 MEM MB DATA36
		DQ36	201 MEM MB DATA37
		DQ37	206 MEM MB DATA38
		DQ38	207 MEM MB DATA39
		DQ39	
			90 MEM MB DATA40
		DQ40	91 MEM MB DATA41
		DQ41	96 MEM MB DATA42
		DQ42	97 MEM MB DATA43
		DQ43	209 MEM MB DATA44
		DQ44	210 MEM MB DATA45
		DQ45	215 MEM MB DATA46
		DQ46	216 MEM MB DATA47
		DQ47	
			99 MEM MB DATA48
		DQ48	100 MEM MB DATA49
		DQ49	105 MEM MB DATA50
		DQ50	106 MEM MB DATA51
		DQ51	218 MEM MB DATA52
		DQ52	219 MEM MB DATA53
		DQ53	224 MEM MB DATA54
		DQ54	225 MEM MB DATA55
		DQ55	
			108 MEM MB DATA56
		DQ56	109 MEM MB DATA57
		DQ57	114 MEM MB DATA58
		DQ58	116 MEM MB DATA59
		DQ59	227 MEM MB DATA60
		DQ60	228 MEM MB DATA61
		DQ61	233 MEM MB DATA62
		DQ62	234 MEM MB DATA63
		DQ63	
			39 MEM MB CHECK0
		CB0	40 MEM MB CHECK1
		CB1	45 MEM MB CHECK2
		CB2	46 MEM MB CHECK3
		CB3	158 MEM MB CHECK4
		CB4	159 MEM MB CHECK5
		CB5	164 MEM MB CHECK6
		CB6	165 MEM MB CHECK7
		CB7	
			126 ✕
		DQS9	135 ✕
		DQS10	144 ✕
		DQS11	153 ✕
		DQS12	204 ✕
		DQS13	213 ✕
		DQS14	222 ✕
		DQS15	231 ✕
		DQS16	162 ✕
		DQS17	

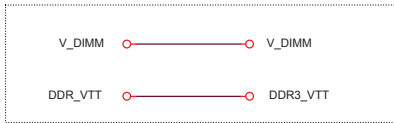
SMBus Addressing

	SMBus 0
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A1

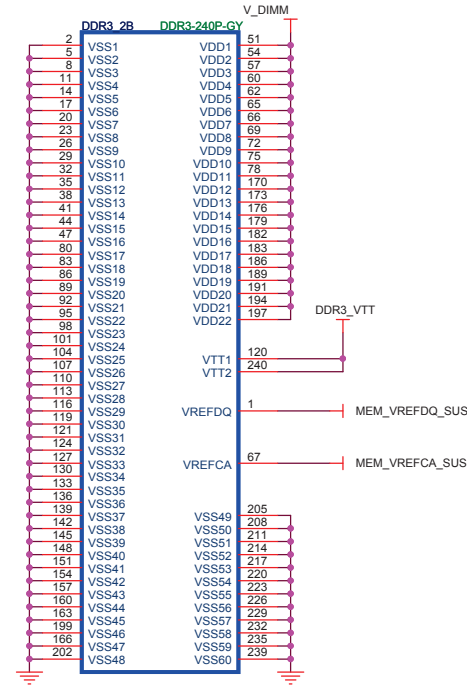
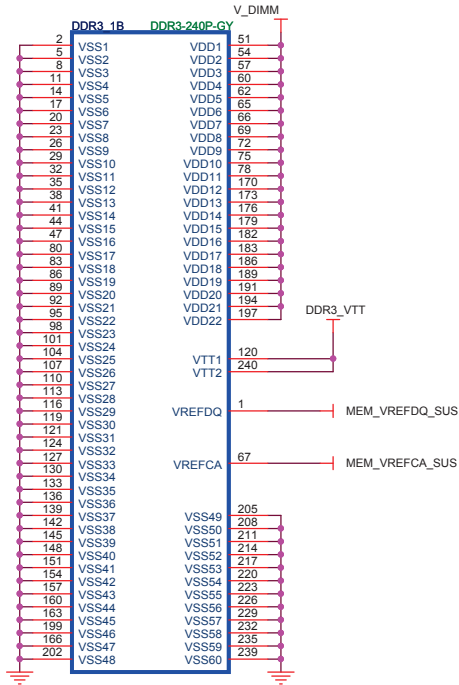
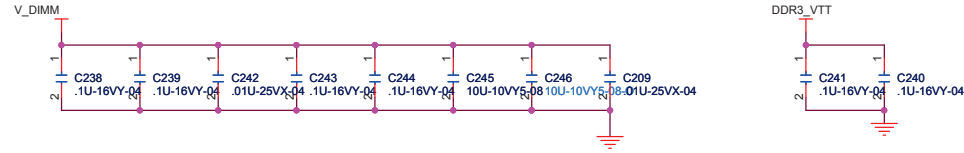
DDR3 DIMM CHANNEL

Size Custom Document Number **A960M-MV** Rev 1.0A

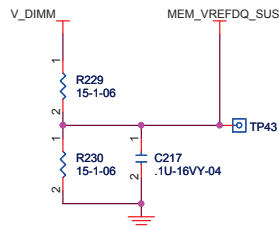
Date: Thursday, October 11, 2012 Sheet 7 of 32



DE-COUPLING CAP FOR DIMMs

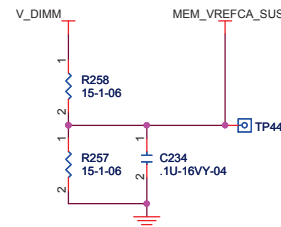


MEM_VREFDQ_SUS

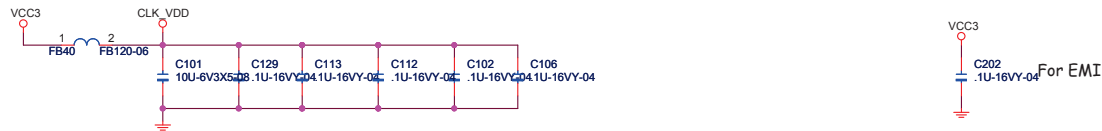


Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width):20mil(spacing)

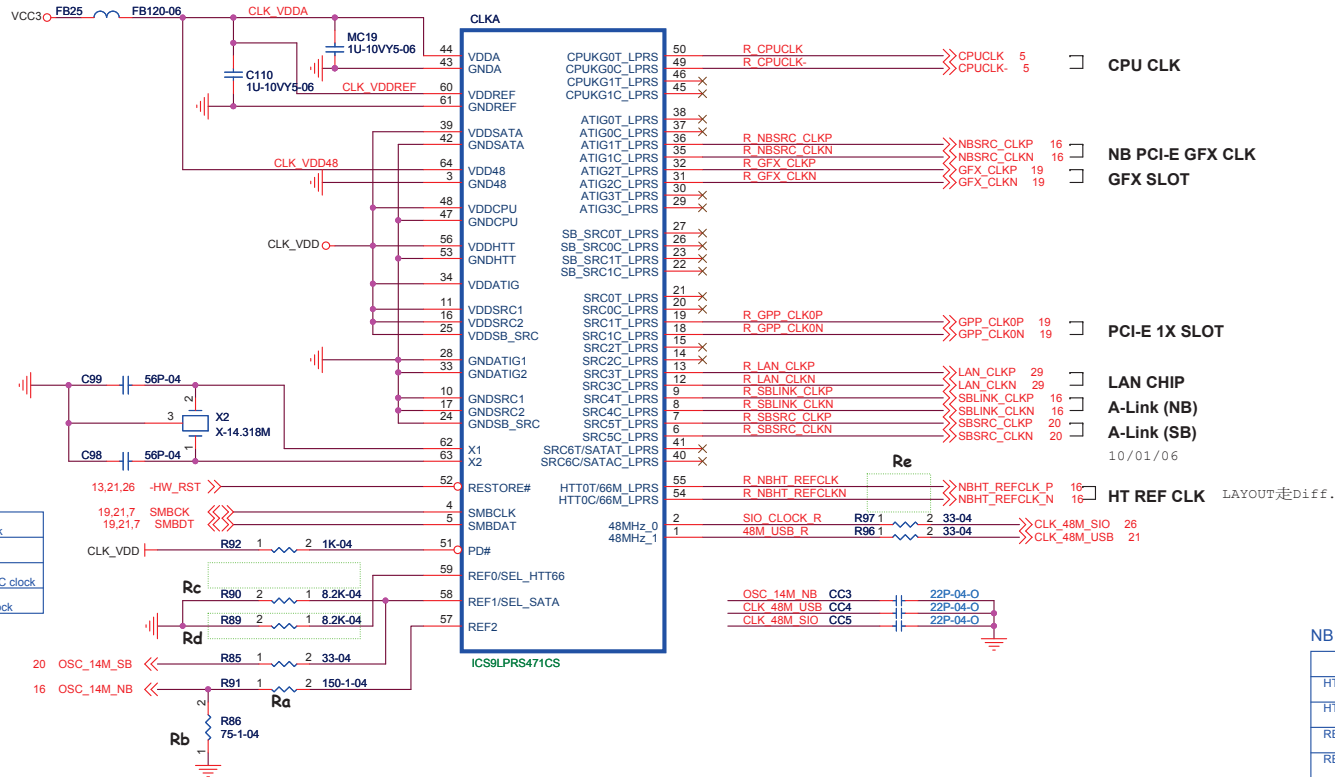
MEM_VREFCA_SUS



Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width):20mil(spacing)



- 1- PLACE ALL SERIAL TERMINATION
RESISTORS CLOSE TO CLOCK GEN
- 2- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



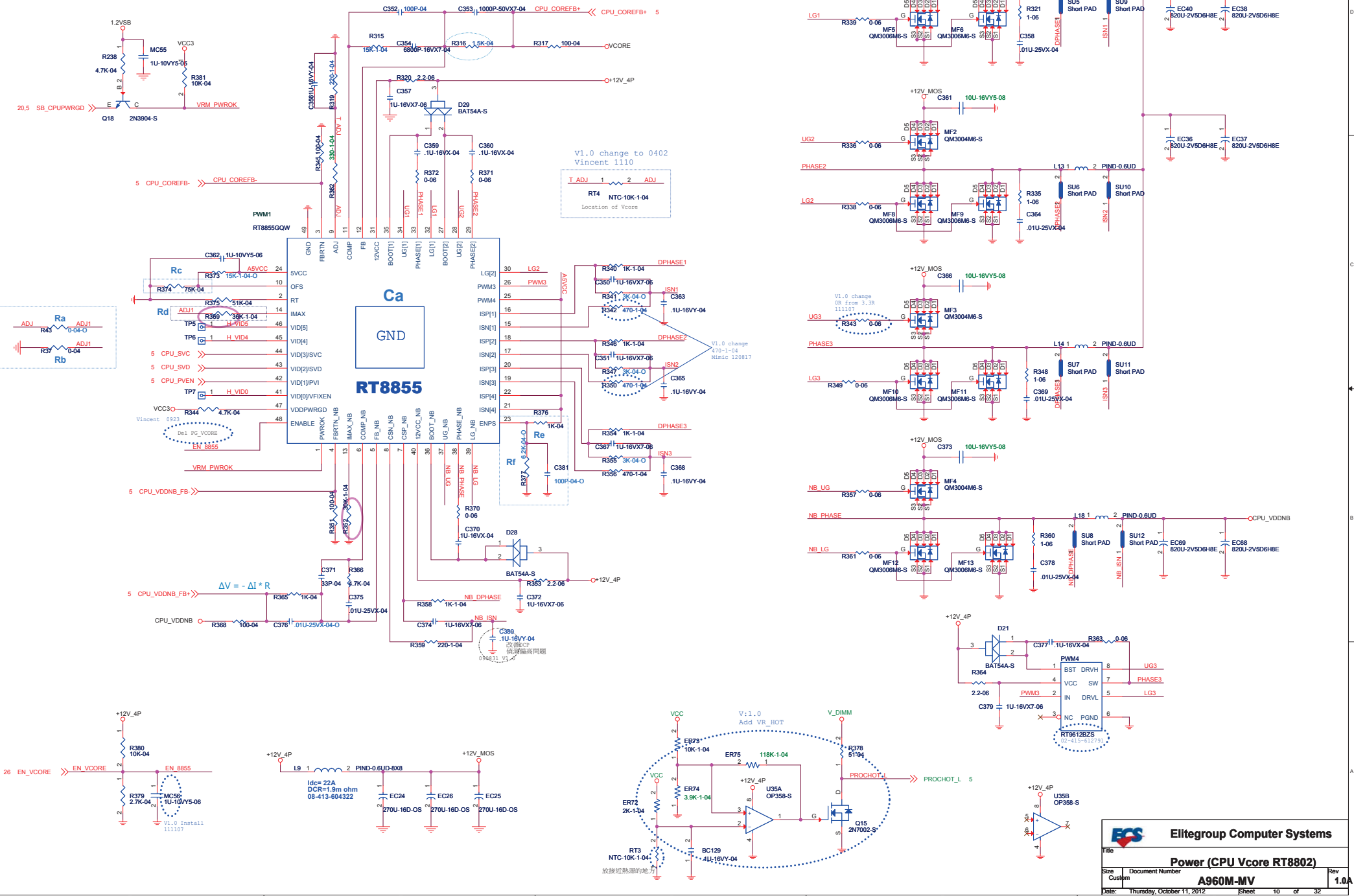
NB CLOCK INPUT TABLE

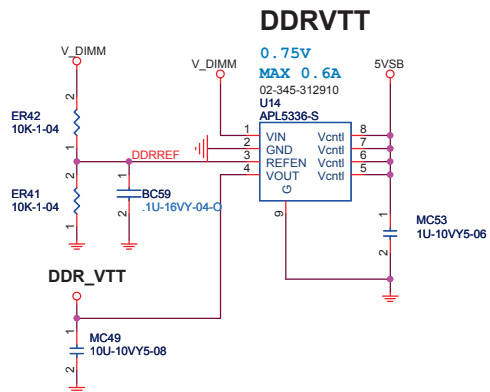
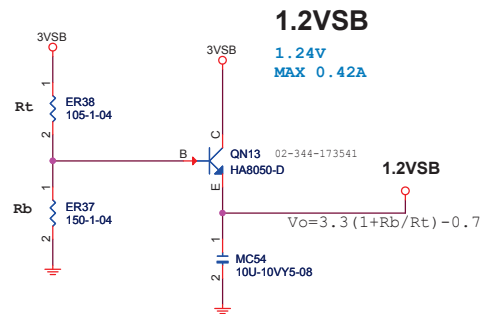
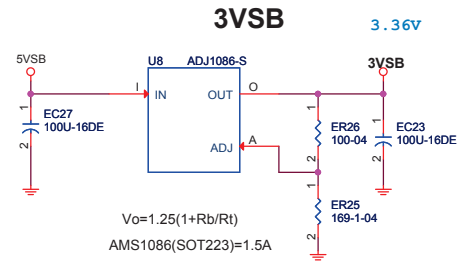
NB CLOCKS	RS740	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF
HT_REFCLKN	NC	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF

* RS880 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.
Clock chip has internal serial terminations for differential pairs

BOM Difference

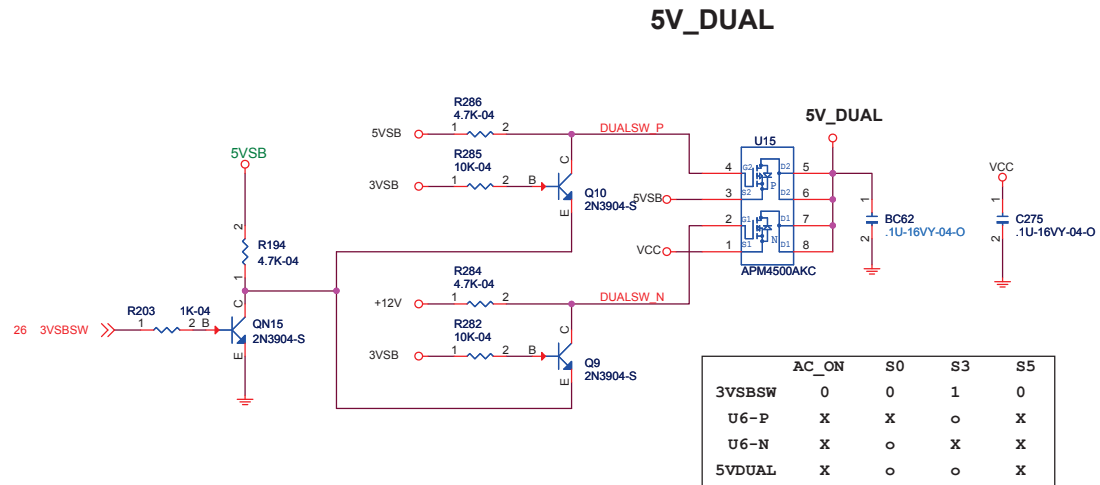
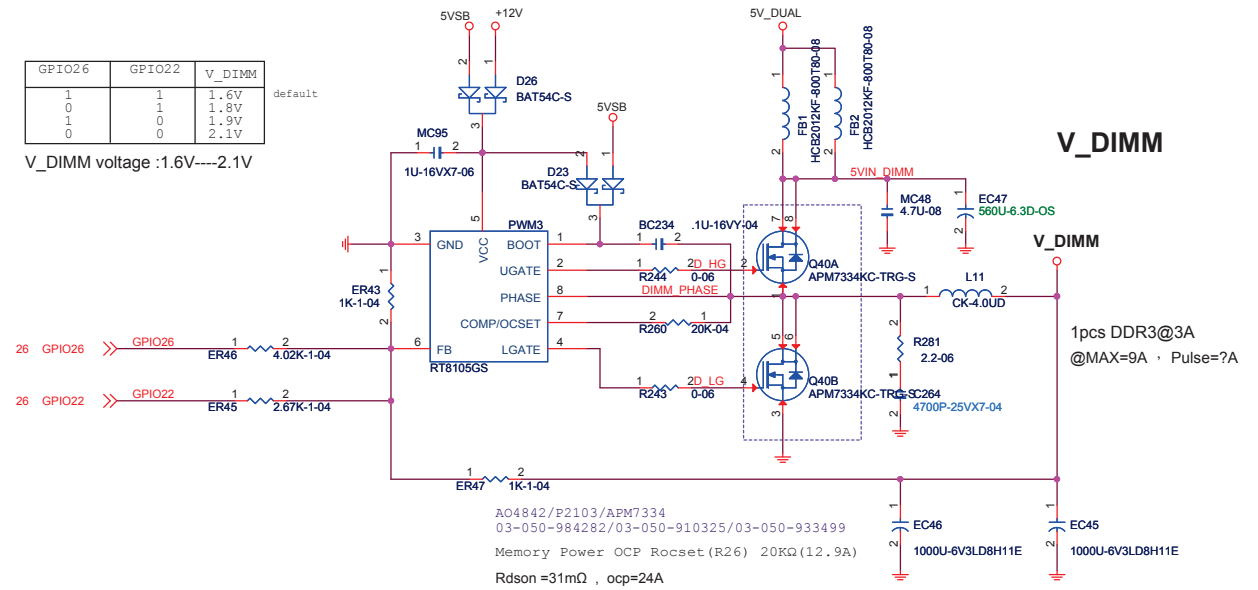
Location	Ca	Ra	Rb	Rc	Rd	Re	Rf
RT8855	RT8855	NC	0-04	75K-04	36K-1-04	1K-04	NC
RT8861	RT8861	0-04	NC	75K-04	7-1-04	30K-1-04	6.2K-04

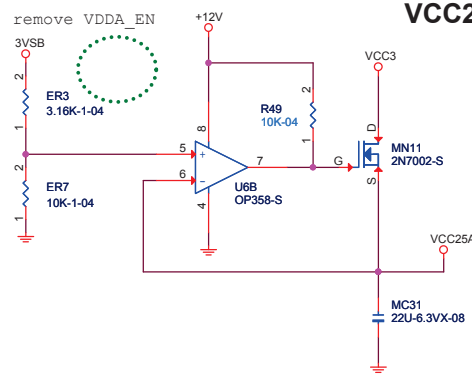
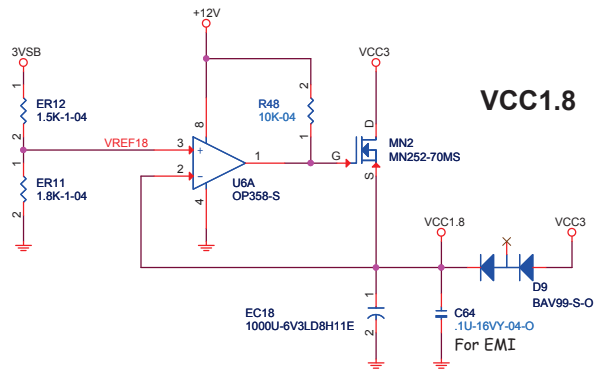




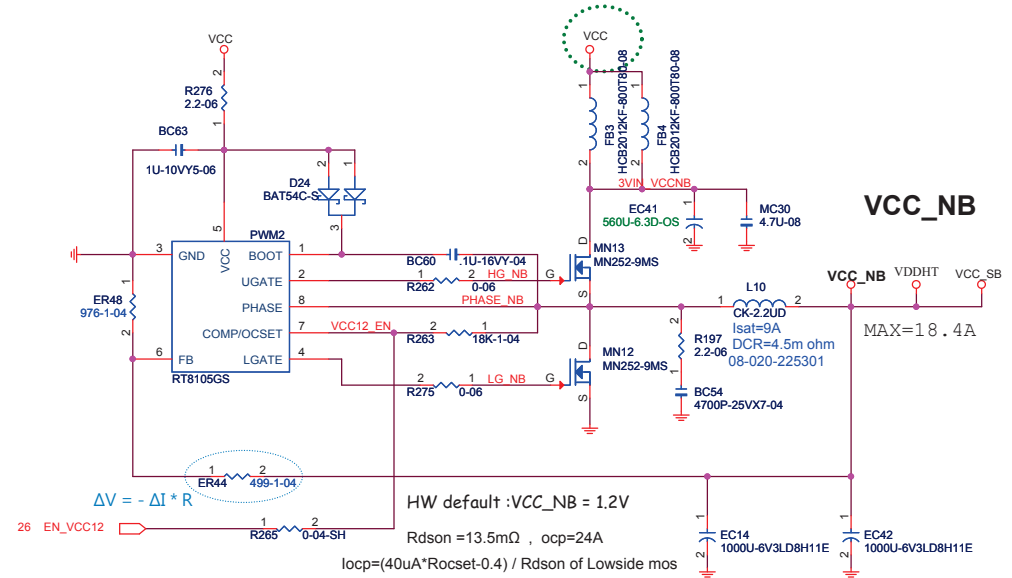
GPIO26	GPIO22	V_DIMM	default
1	1	1.6V	
0	1	1.8V	
1	0	1.9V	
0	0	2.1V	

V_DIMM voltage :1.6V----2.1V

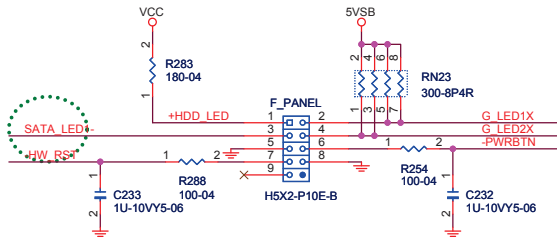
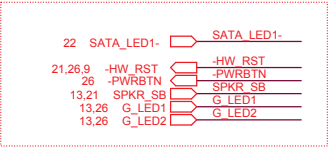




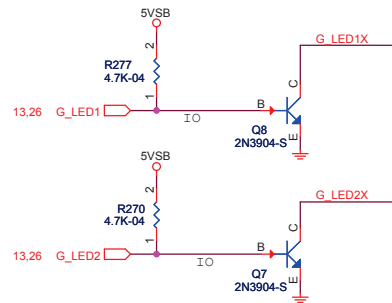
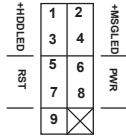
Near CPU.



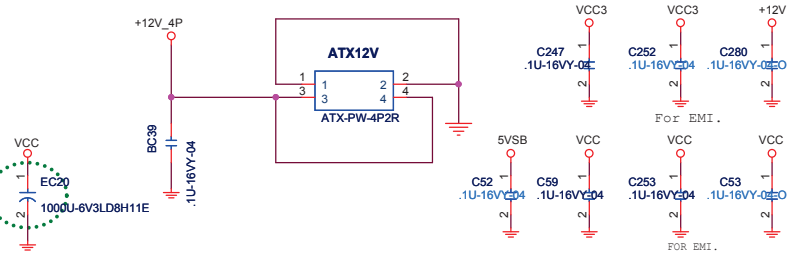
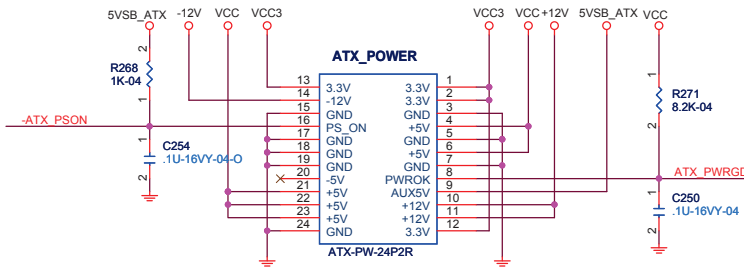
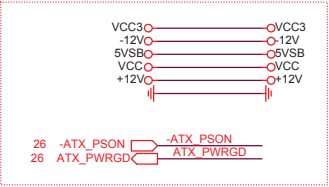
FRONT PANEL
External Connection



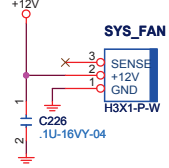
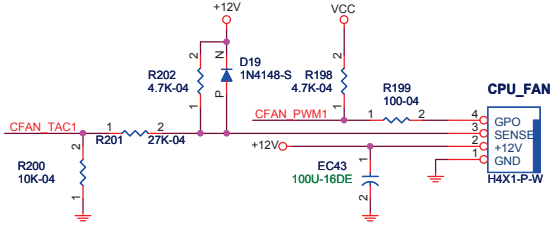
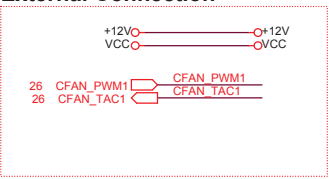
F_PANEL



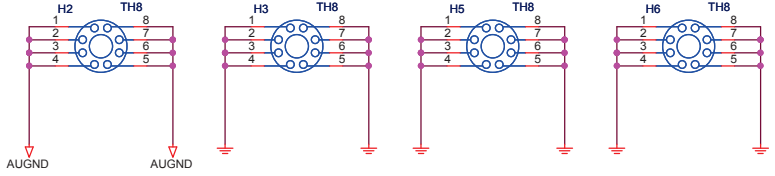
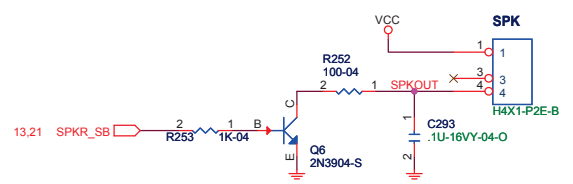
POWER CONNECTOR
External Connection



FAN
External Connection

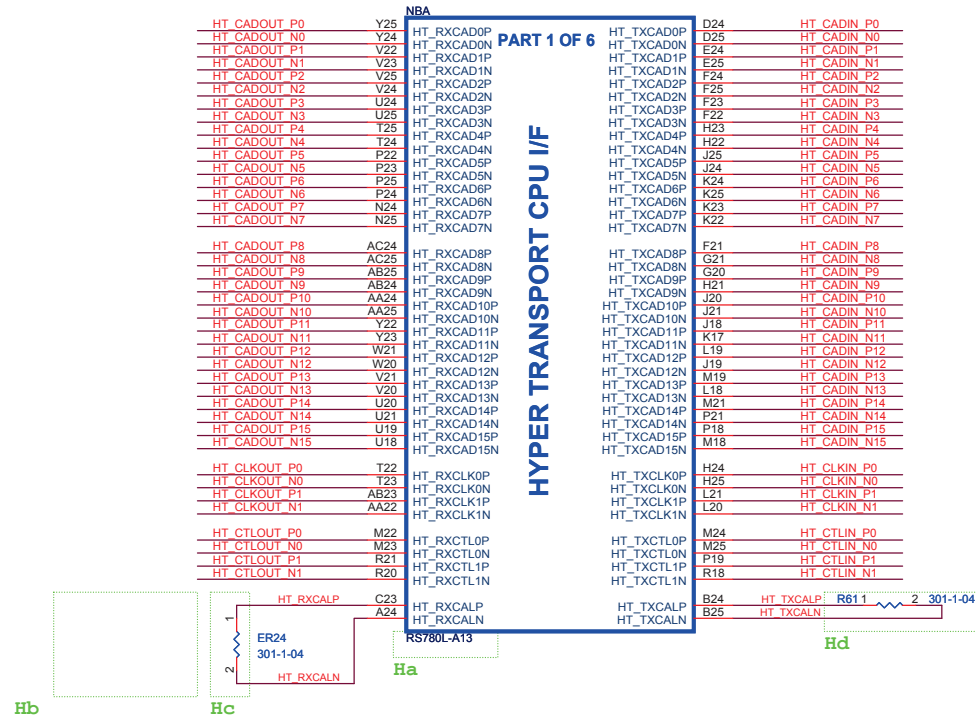


BUZZER



HT LINK

3 HT_CLKIN_H[0..1]	>>	HT_CLKIN_P[0..1]
3 HT_CLKIN_L[0..1]	>>	HT_CLKIN_N[0..1]
3 HT_CLKOUT_H[0..1]	<<	HT_CLKOUT_P[0..1]
3 HT_CLKOUT_L[0..1]	<<	HT_CLKOUT_N[0..1]
3 HT_CADIN_H[0..15]	>>	HT_CADIN_P[0..15]
3 HT_CADIN_L[0..15]	>>	HT_CADIN_N[0..15]
3 HT_CADOUT_H[0..15]	<<	HT_CADOUT_P[0..15]
3 HT_CADOUT_L[0..15]	<<	HT_CADOUT_N[0..15]
3 HT_CTLIN_H[0..1]	>>	HT_CTLIN_P[0..1]
3 HT_CTLIN_L[0..1]	>>	HT_CTLIN_N[0..1]
3 HT_CTLOUT_H[0..1]	<<	HT_CTLOUT_P[0..1]
3 HT_CTLOUT_L[0..1]	<<	HT_CTLOUT_N[0..1]



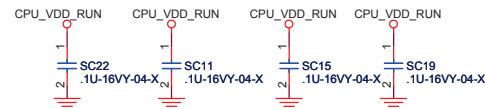
01-201-780240 IC NB.RS780L A13.FCBGA 528P.HDMI
RS740/RS760/RS780 difference BOM table (HT LINK)

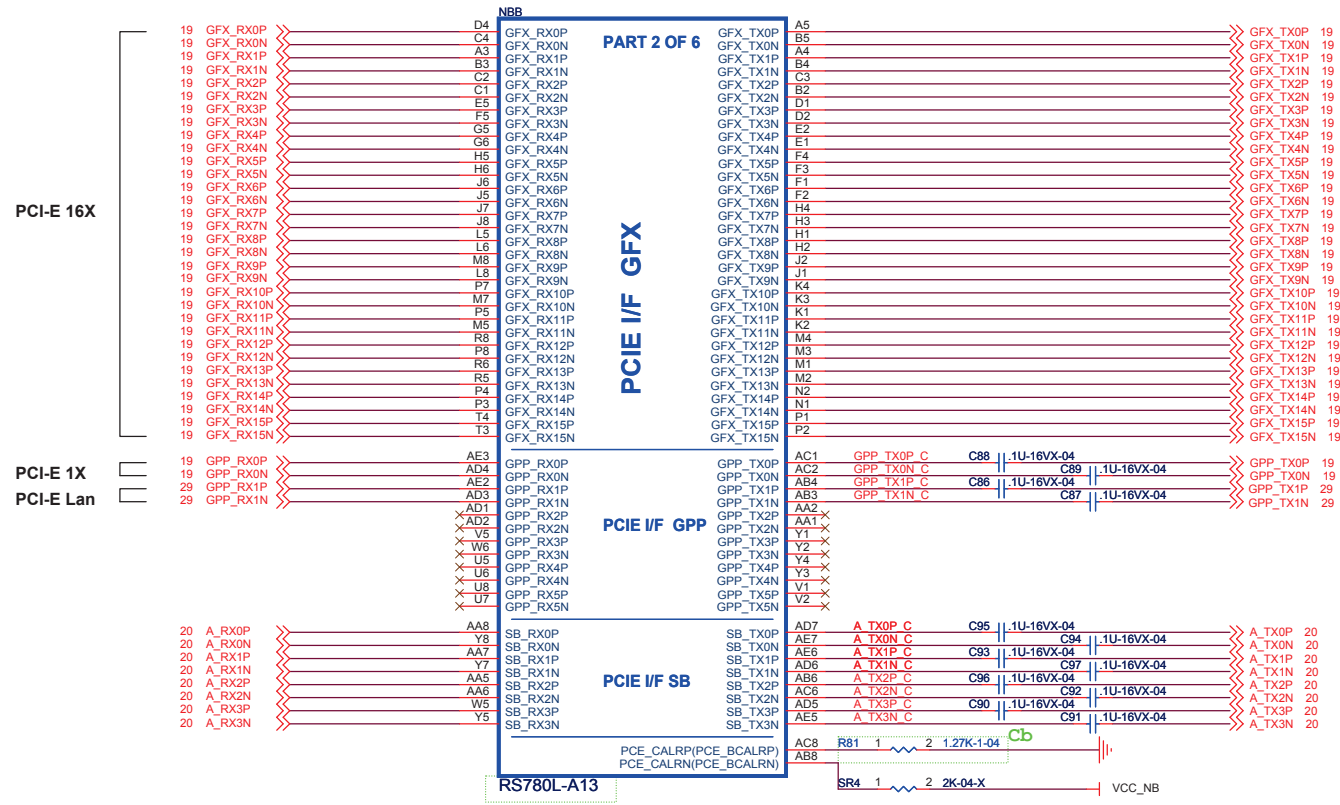
	RS740	RS780-A13
Ha	RS740	RS780-A13
Hb	V	X
Hc	X	V
Hd	100-04	301-1-04

RX780/RS740/RS780 difference table (HT LINK)

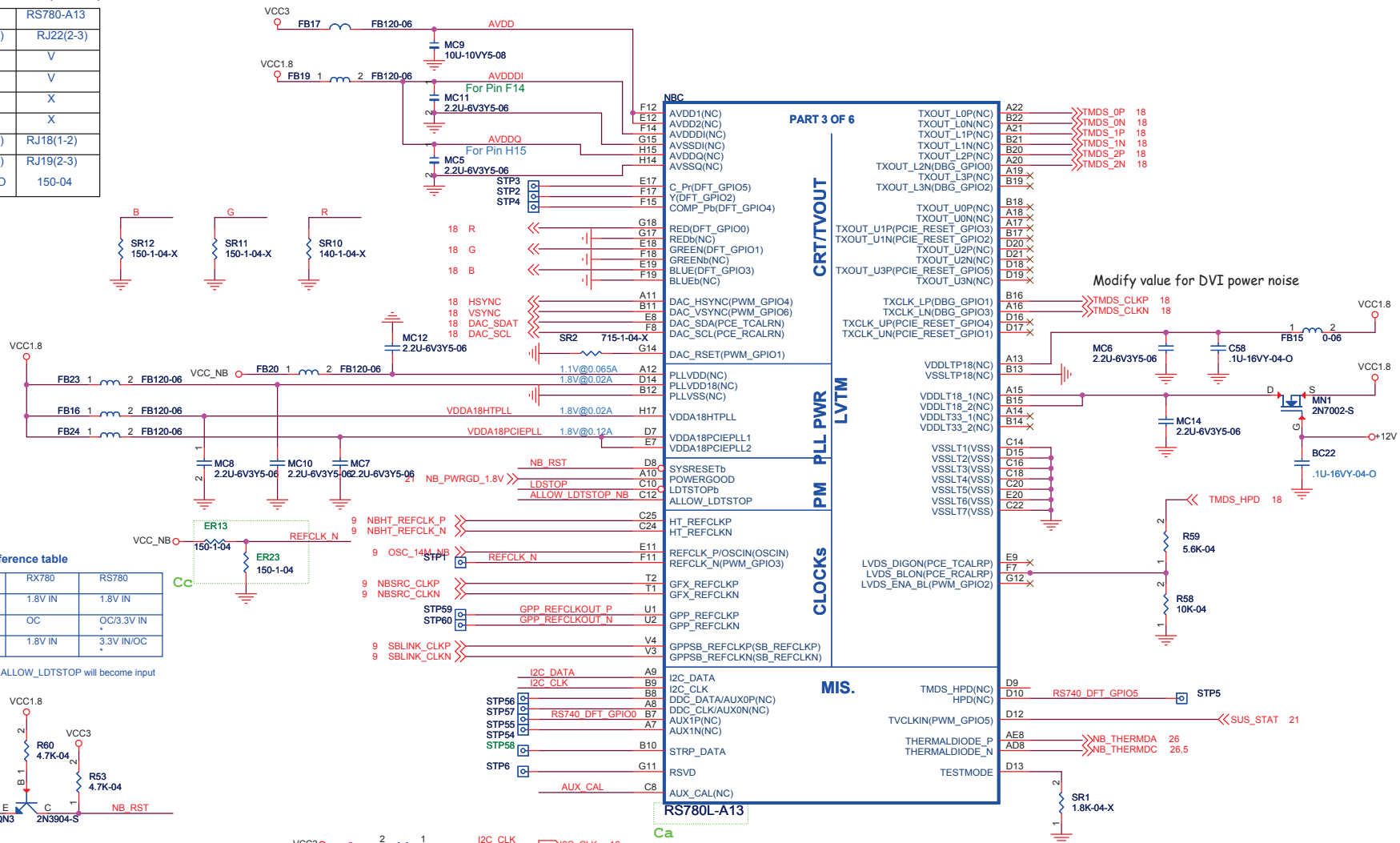
SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)		
HT_RXCALN	49.9R (VDDHT)	1.21K	301R
HT_TXCALP	100R *	1.21K	301R
HT_TXCALN			

TX signals return path CAP , Placed near the North Bridge





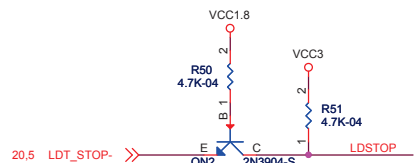
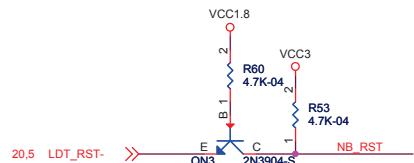
Ca	RS740	RS780-A13
Cb	RJ22(1-2)	RJ22(2-3)
Cc	X	V
Cd	X	V
Ce	V	X
Cf	V	X
Cg	RJ18(2-3)	RJ18(1-2)
Ch	RJ19(1-2) 2.2K-04-O	RJ19(2-3) 150-04



RX740/RS740/RS780 difference table

	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN *
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC *

*. CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input



NB output is OD pin

RS740: STRAP_DEBUG_BUS_GPIO_ENABLE

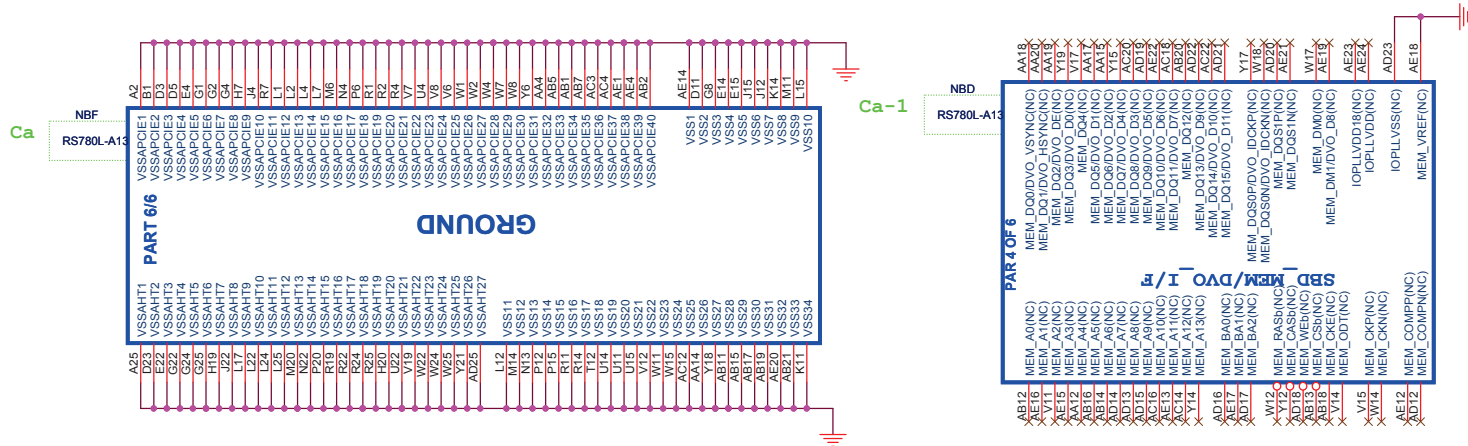
Enables the Test Debug Bus using GPIO.
1 : Disable
0 : Enable

RS740: Enables Side port memory

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]

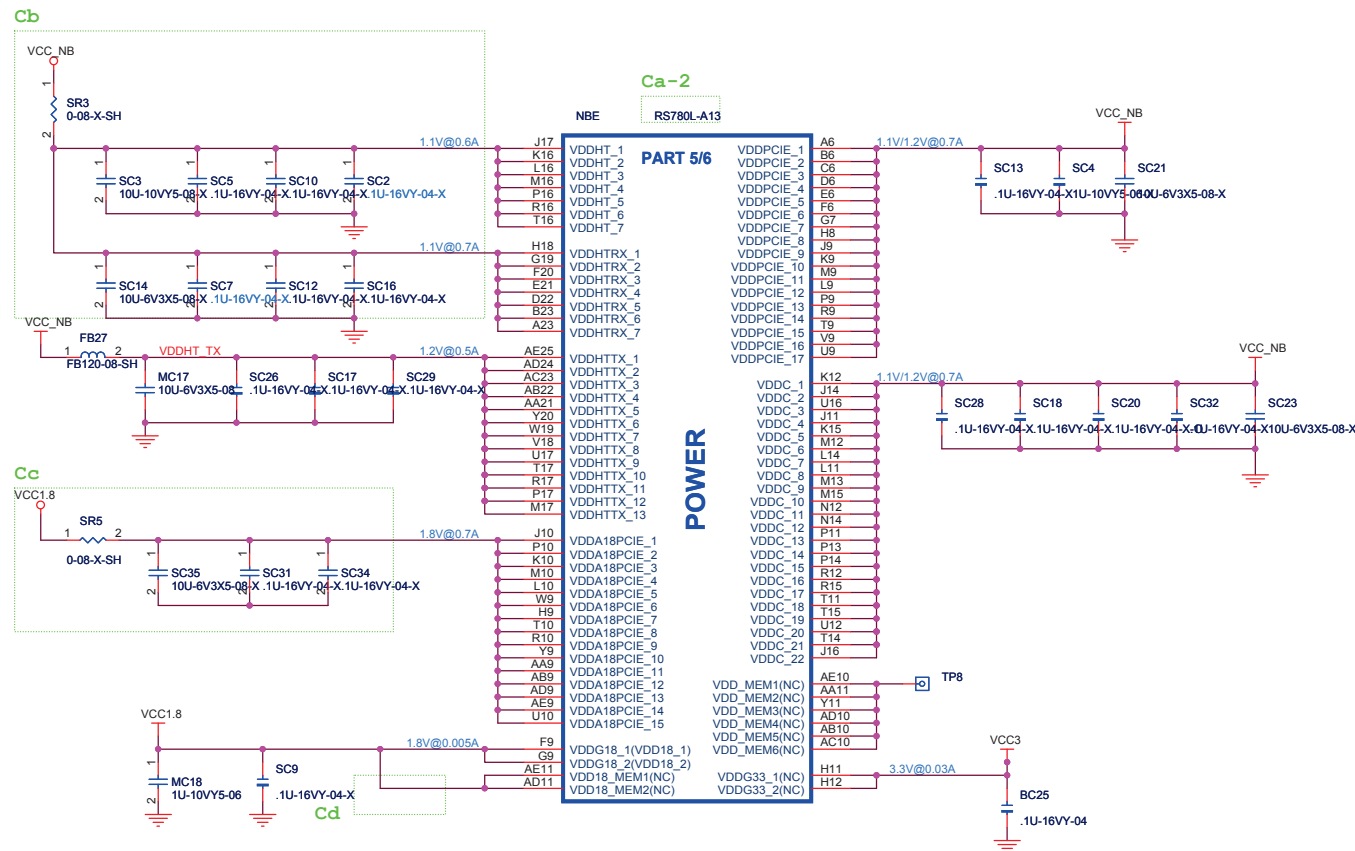
RS740: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



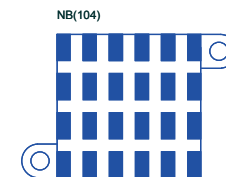
RS740 POWER DIFFERENCE TABLE

PIN NAME	RS740	RS780	PIN NAME	RS740	RS780
VDDHT	NC	+1.1V	IOPLLVD	+1.2V	+1.1V
VDDHTRX	NC	+1.1V	AVDD	+3.3V	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	+1.8V	+1.8V
VDDA18PCIE	NC	+1.8V	AVDDQ	+1.8V	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	+1.2V	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	+1.8V	+1.8V
VDDPCIE	+1.2V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V
VDDC	+1.2V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	+1.8V/1.5V	VDDLTP18	+1.8V	+1.8V
VDDG33	+3.3V	+3.3V	VDDLTP18	+1.8V	+1.8V
IOPLLVD18	+1.8V	+1.8V	VDDLTP18	+3.3V	NC



RS740/RS760/RS780 difference BOM table (HT LINK)

	Ca	RS740	RS780-A13
Ca-1		RS740	RS780-A13
Ca-2		RS740	RS780-A13
Cb		X	V
Cc		X	V
Cd		X	V

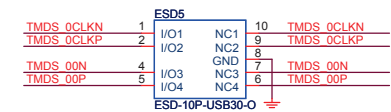
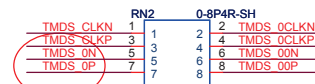
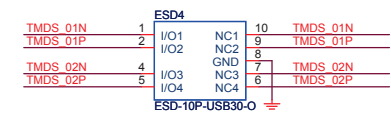
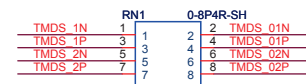
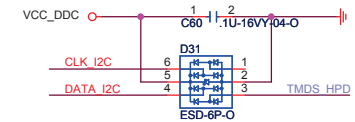
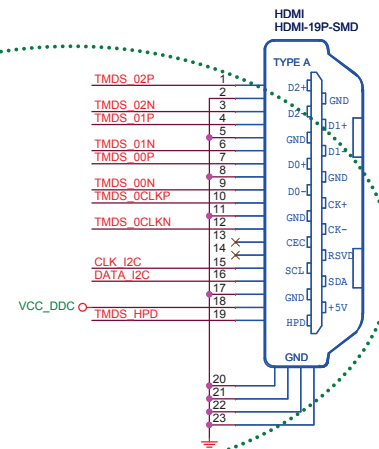
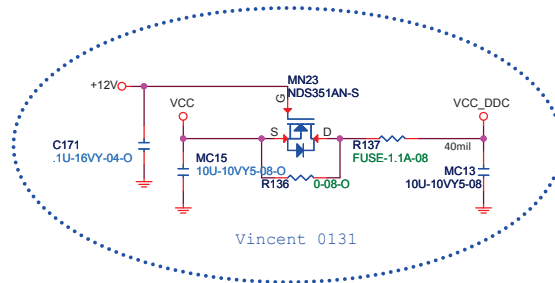
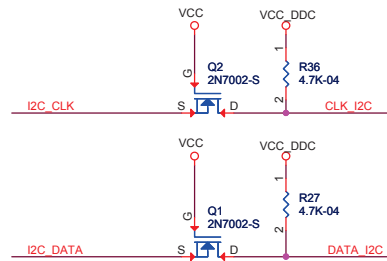
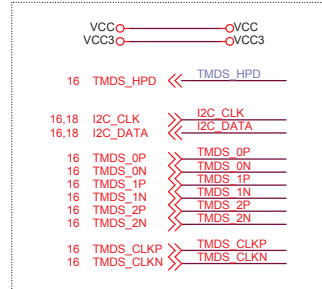


20-120-020456

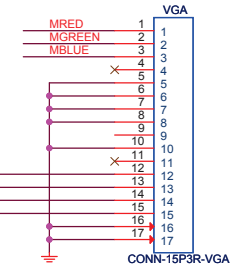
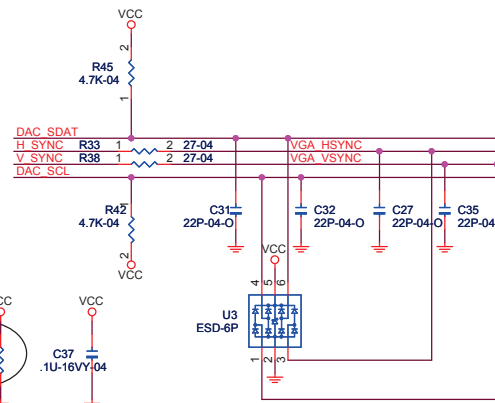
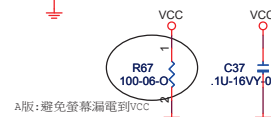
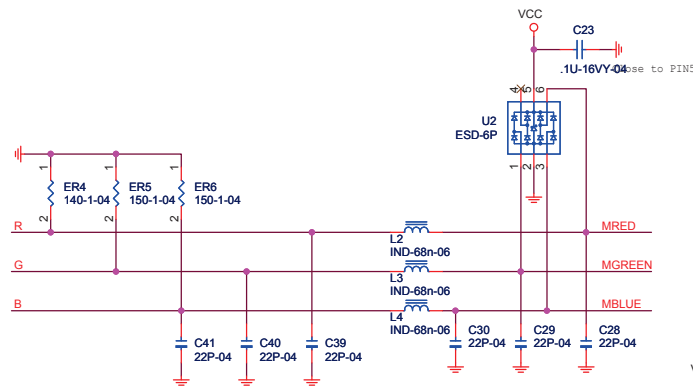
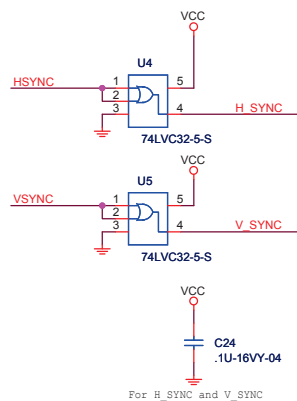
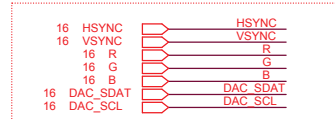
NB (104)

20-120-020456/20-120-020457

External Connection

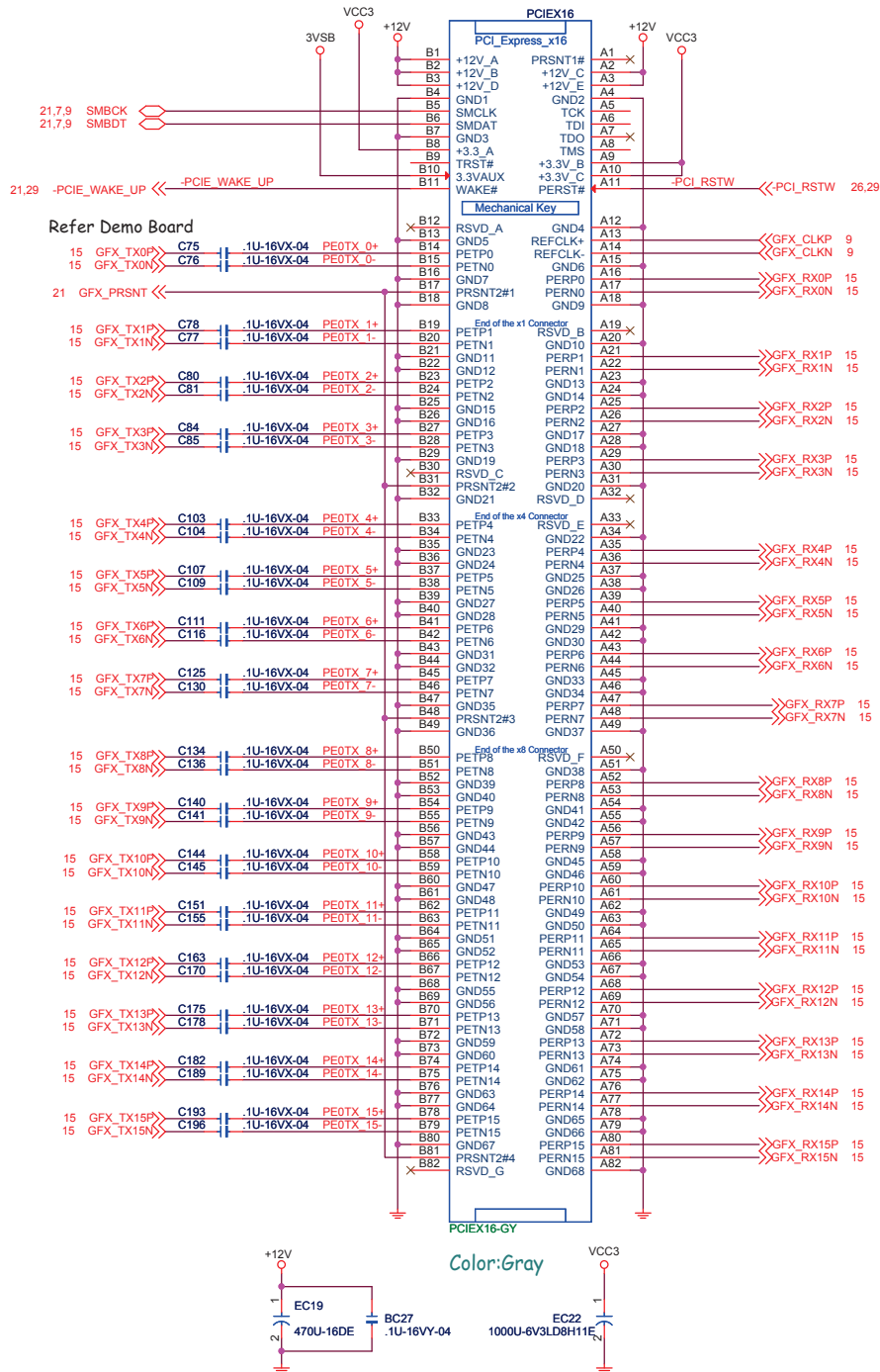


External Connection



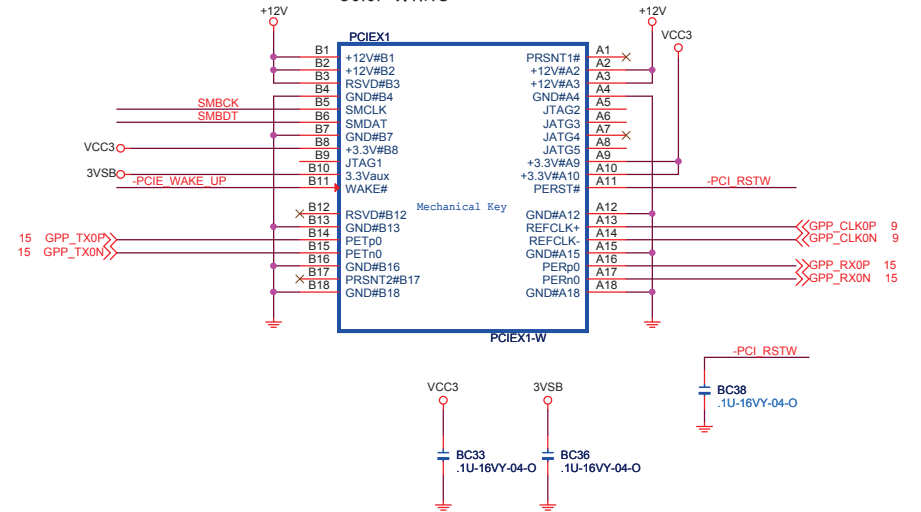
PCI_EXPRESS_x16

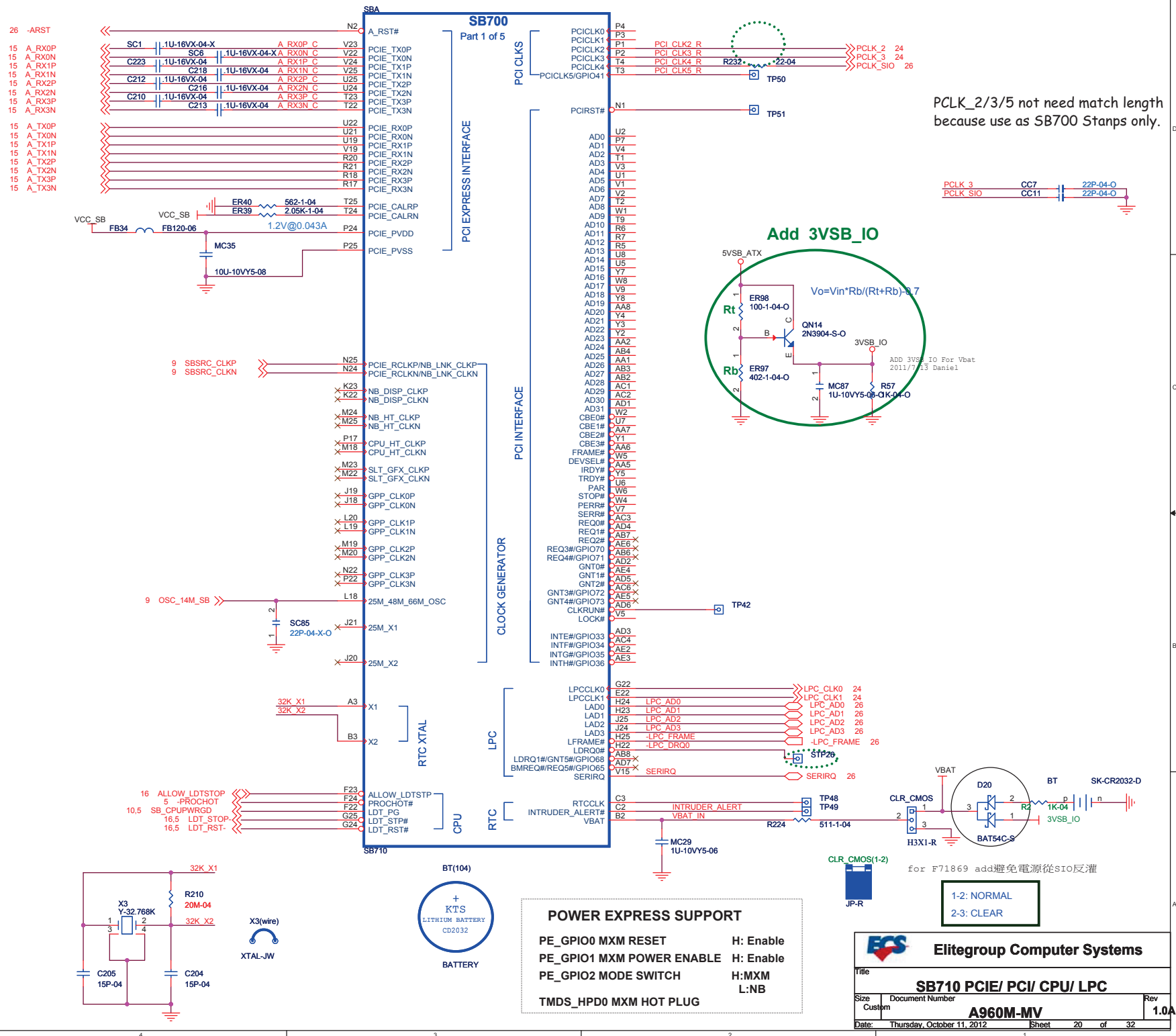
+12V: 5.5Amp

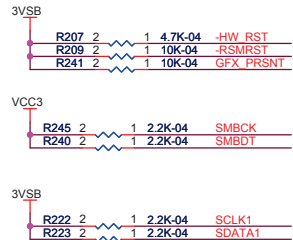


PCI_EXPRESS_x1

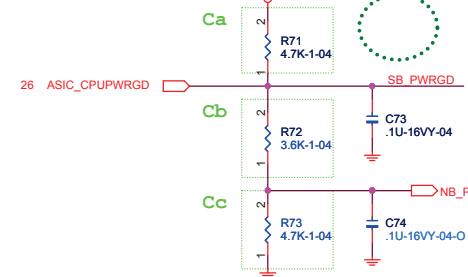
Color: White





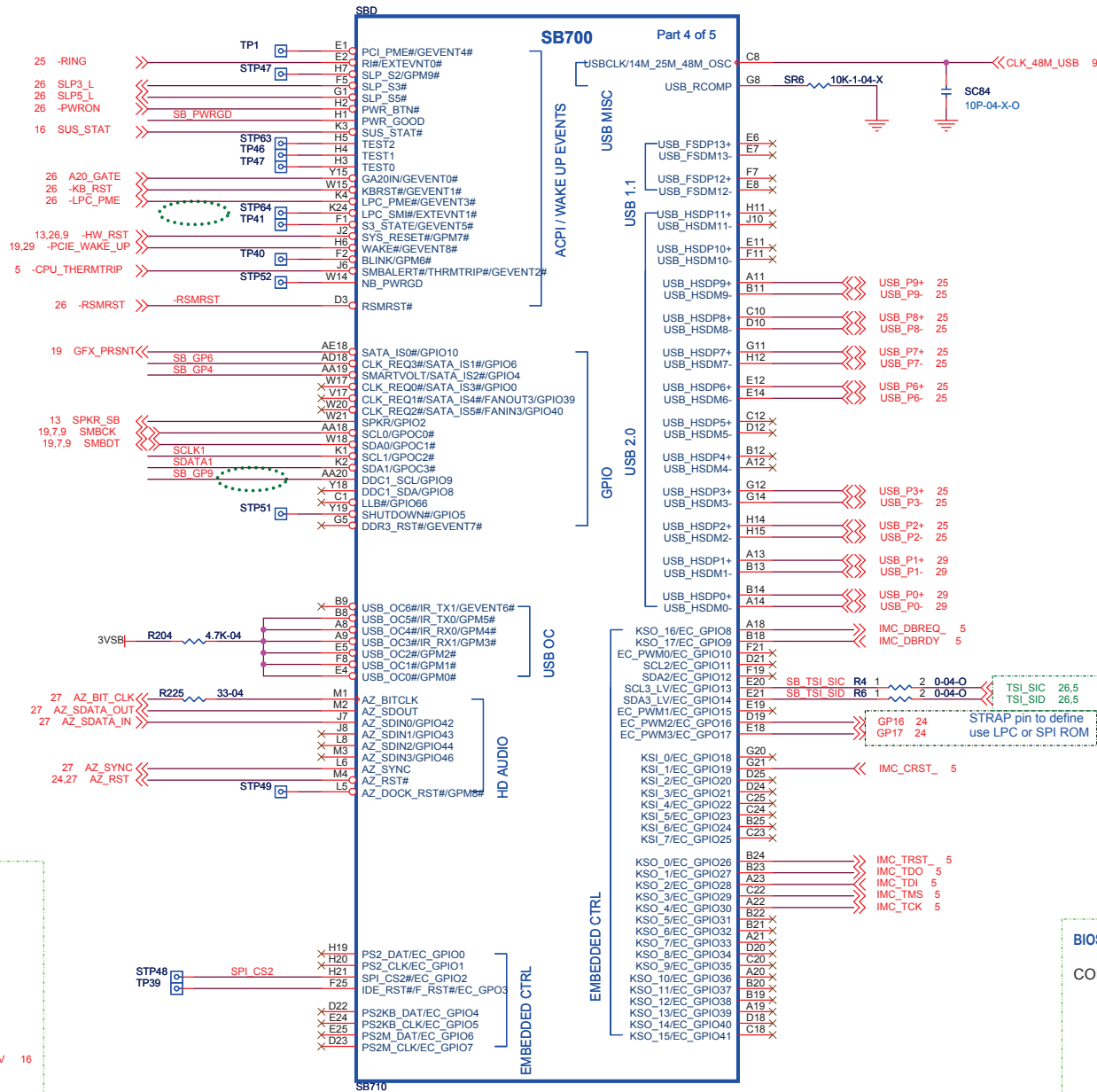


SB&NB PWRGOOD

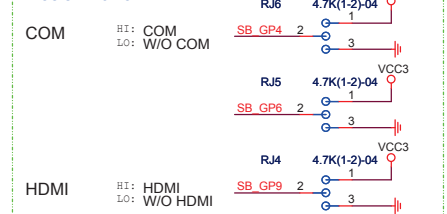


RS740/RS760/RS780 difference BOM table

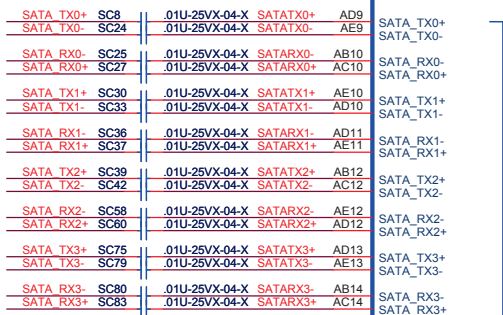
	RS740	RS780-A13
Ca	5.1K-1-04	4.7K-1-04
Cb	0-04	3.6K-1-04
Cc	10K-1-04	4.7K-1-04



BIOS SELECTION



**PLACE SATA AC COUPLING
CAPS CLOSE TO SB710**



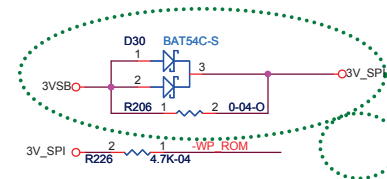
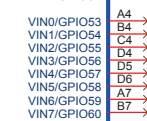
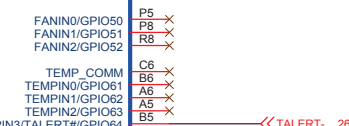
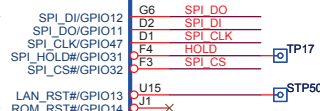
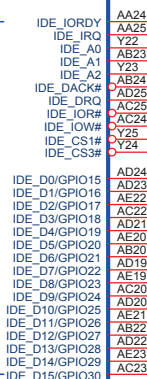
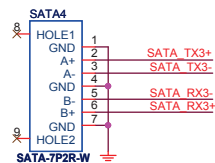
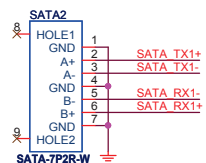
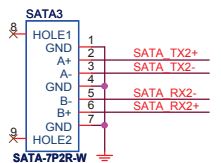
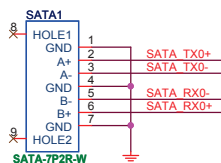
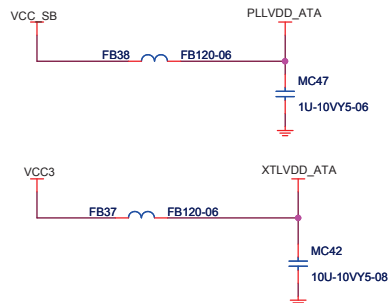
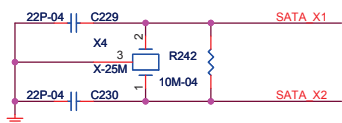
SB700
Part 2 of 5



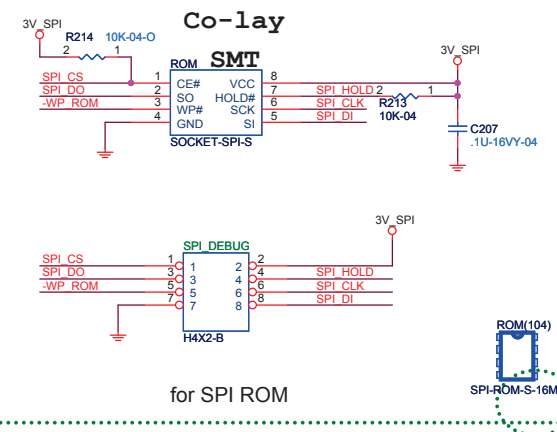
**PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700**

NOTE :
SR2 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

NOTE :
SR2 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

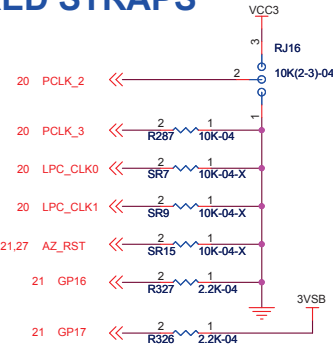


Vincent 0207



NOTE: SB710 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

REQUIRED STRAPS



SB710 POWER TABLE

PIN NAME	SB710	PIN NAME	SB710
VCC_SB: 1.2V		VCC3	
PCIE_PVDD	0.043A	XTLVDD SATA	0.006A
PLLVDVDD SATA	0.093A	VDDQ	0.131A
PCIE_VDDR	0.6A	VDD33_18	0.071A
AVDD SATA	0.567A	AVDDCK 3.3V	0.047A
VDD	0.51A	Total	0.255A
CKVDD 1.2V		3VSB	
AVDDCK 1.2V	0.062A	AVDDTX/RX	0.658A
Total	1.875A	AVDDC	0.017A
1.2VSB		S5_3.3V	0.032A
S5_1.2V	0.113A	Total	0.707A
USB_PHY 1.2V		5VSB	
USB_PHY 1.2V	0.197A	V5_VREF	0.001A
Total	0.31A		



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	Watchdog ENABLED DEFAULT	USE DEBUG STRAPS	RESERVED	RESERVED	IMC Enable	CLKGEN ENABLED	INTERNAL RTC DEFAULT	PCI ROM BOOT Enable	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	Watchdog DISABLED	IGNORE DEBUG STRAPS DEFAULT			IMC Disable DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	PCI ROM BOOT Disable DEFAULT	L, H = LPC ROM L, L = FWH ROM	

A12

A12



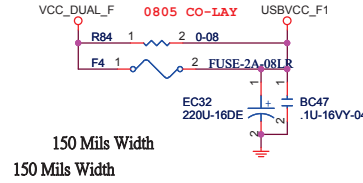
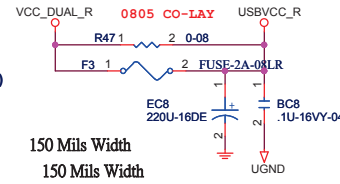
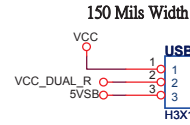
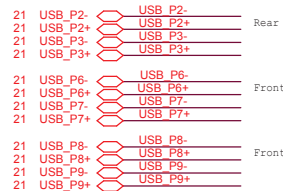
Remove LPT

Remove IDE



External Connection

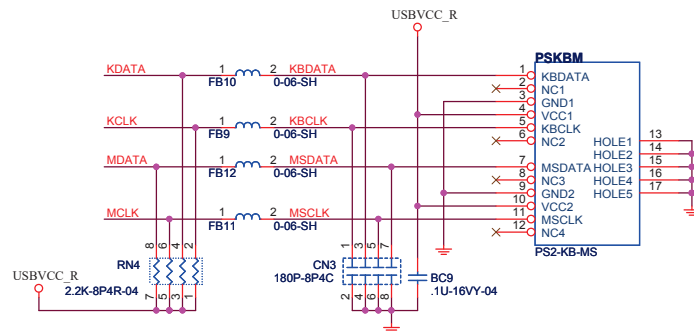
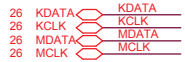
VCC
USBVCC_R



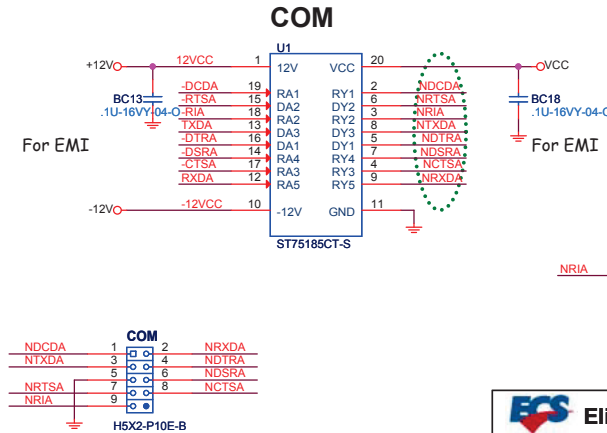
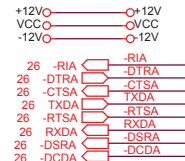
USBPWR_R1	USB POWER SELECT
1-2	VCC *
2-3	5VSB



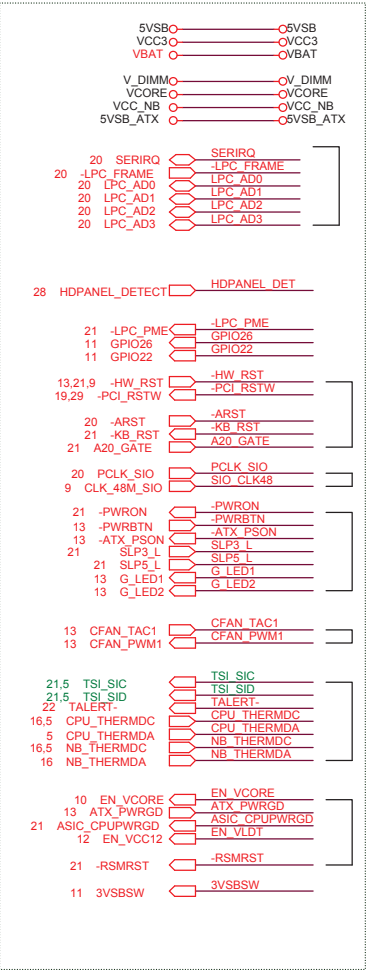
PSKBM External Connection



COM Ports External Connection



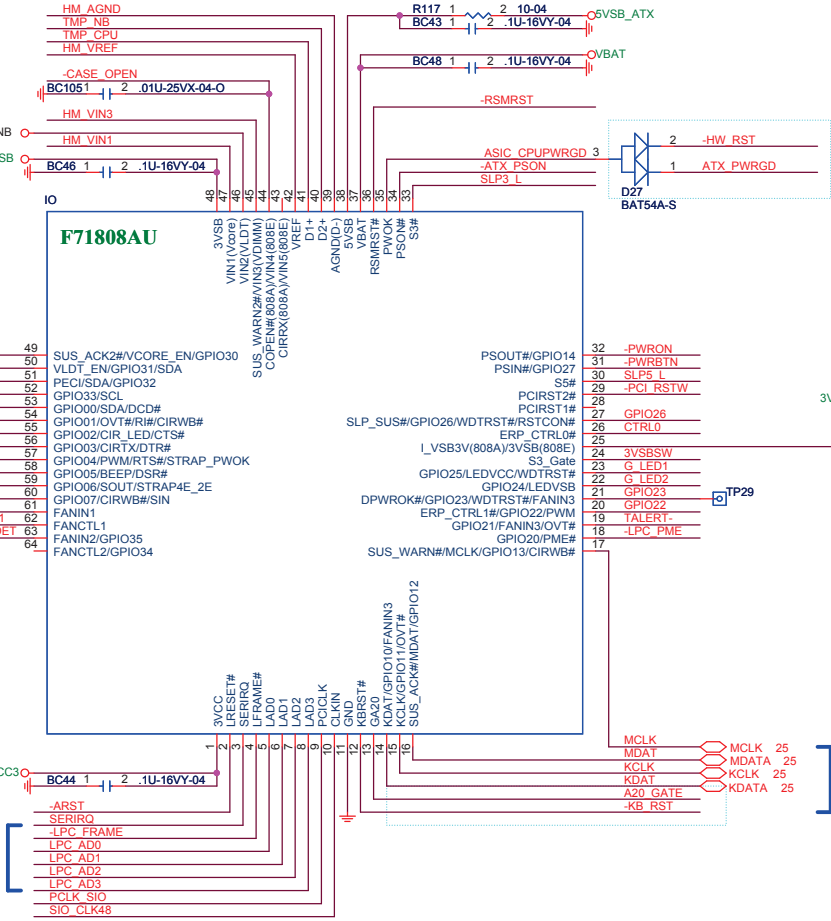
External Connection



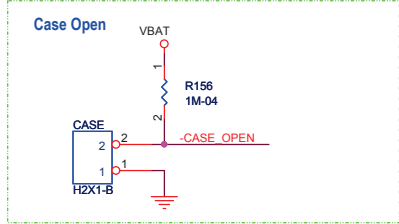
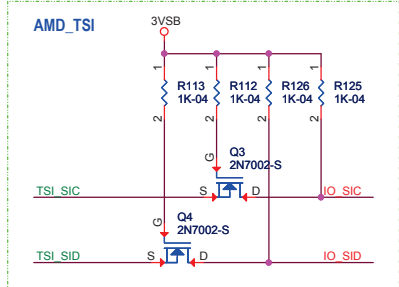
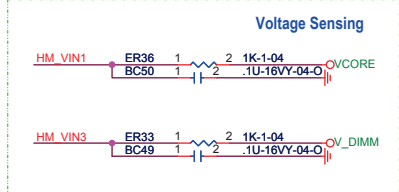
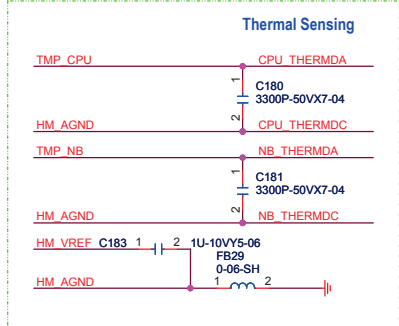
COM

- EN_VCORE
- IO_SID
- IO_SIC
- DCDA
- RIA
- CTSA
- DTRA
- RTSA
- DSRA
- TXDA
- RXDA
- CFAN_TAC1
- CFAN_PWM1
- TSI_SIC
- TSI_SID
- TALERT
- CPU_THERMDC
- CPU_THERMDA
- NB_THERMDC
- NB_THERMDA
- EN_VCORE
- ATX_PWRGD
- ASIC_CPU_PWRGD
- EN_VCC12
- RSMRST
- 3VBSW

LPC



KB / MS

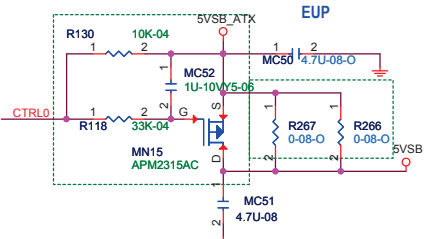
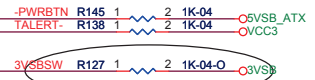


Power On Strapping

(PIN 59)
(PIN 57)

PIN NO.	Symbol	Value	Description
PIN 59	STRAP4E_2E	1	Configuration Register I/O port is 4E/4F.(Default)
		0	Configuration Register I/O port is 2E/2F.
PIN 57	STRAP_PWOK	1	PWOK(pin 35) for AMD(Default)
		0	PWOK(pin 35) for Intel

Open Drain



Elitegroup Computer Systems

SIO - F71869AU

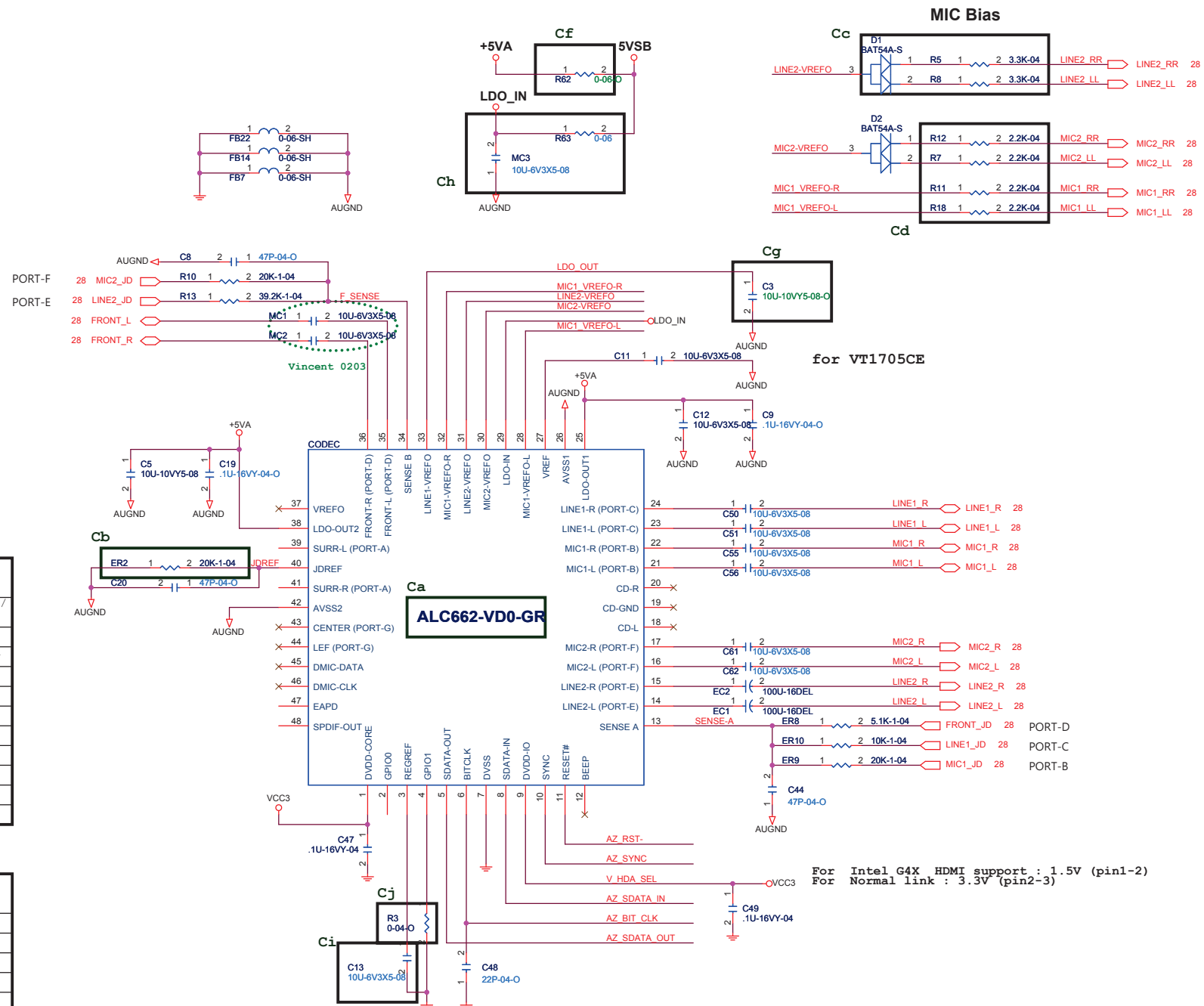
Size Custom Document Number A960M-MV Rev 1.0A

Date: Thursday, October 11, 2012 Sheet 26 of 32

VCC3 ○ ○ VCC3
5VSB ○ ○ 5VSB

21,24 AZ_RST ○ AZ RST-
21 AZ_SYNC ○ AZ SYNC
21 AZ_SDATA_IN ○ AZ SDATA IN
21 AZ_BIT_CLK ○ AZ BIT CLK
21 AZ_SDATA_OUT ○ AZ SDATA OUT

AUGND ◀ ▶ AUGND

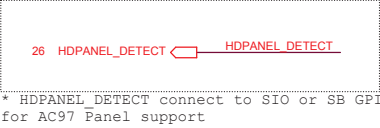


Pin	ALC662VD	VT1705CE	VT1705CF
2	GPIO0	GPIO0/SPDIF_TX1	GPIO0/SPDIF_TX1/ DMIC_CLK
3	REG VREF	GPIO1	REGREF
4	GPIO1	DVSS	GPIO1/DMIC_DATA
25	LDO OUTPUT	LDO VIN	LDO_OUT1
29	LDO VIN	OPTION CAP	LDO_IN
33	LINE1 VREF	LDO OUTPUT	SENSE_C
37	FRONT VREF ?	NC	VREFOUT_C
38	LDO OUTPUT	LDO VIN	LDO_OUT2
45	DMIC DATA	NC	NC
46	DMIC CLK	NC	NC
47	EADP	EADP	EADP/SPIDF_RX

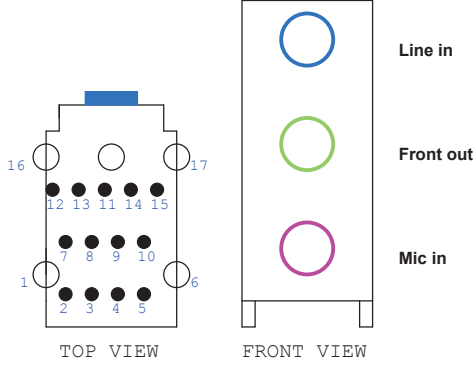
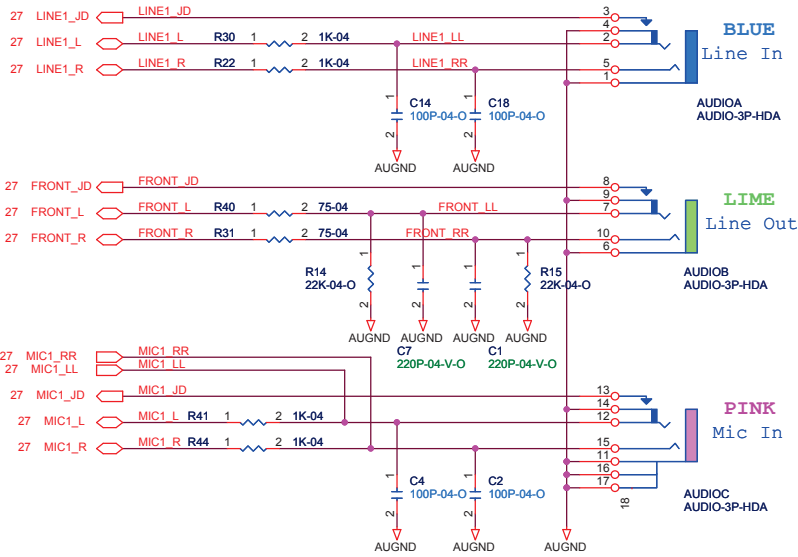
Location	ALC662VD	VT1705CE	VT1705CF
Ca	ALC662-VD0-GR	VT1705CE	VT1705CF
Cb	20K-1-04	5.1K-1-04	20K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	16-04	32-04
Cf	X	V	X
Cg	X	V	X
Ch	V	X	V
Ci	V	X	V
Cj	X	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

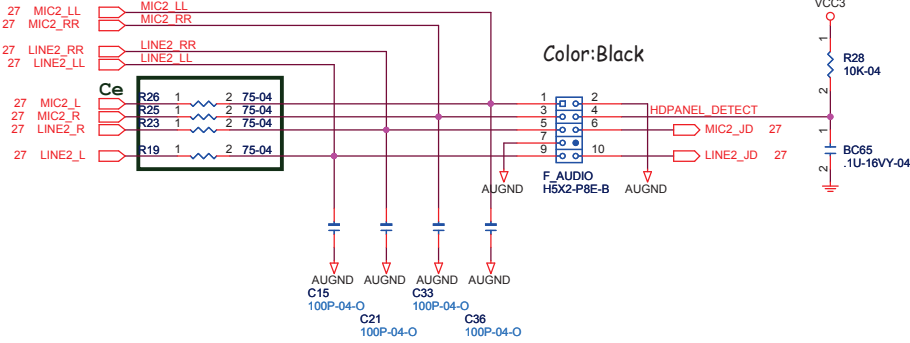
External Connection




REAR-AUDIO



FRONT-AUDIO



 Elitegroup Computer Systems

Title			AUDIO 1705&ALC662 (PANEL)		
Size	Document Number	A960M-MV			Rev
Custom					1.0A
Date:	Thursday, October 11, 2012	Sheet	28	of	32

Pin	Signal
19	USBVCC_R0
20	3VSB
21	VCC3
22	UGND
23	PCIE_WAKE_UP
24	PCIE_LAN1_RST+
25	LAN_CLKP
26	LAN_CLKN
27	GPP_TX1P
28	GPP_TX1N
29	GPP_RX1P
30	GPP_RX1N
31	USB_P0-
32	USB_P0+
33	USB_P1-
34	USB_P1+

VDD1.05_A

Closed To Pin6,9,41

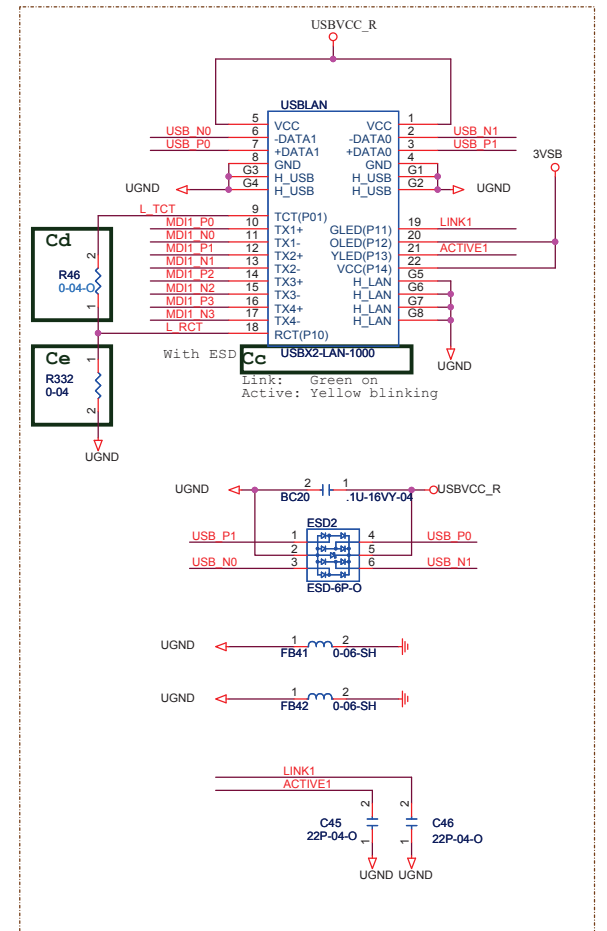
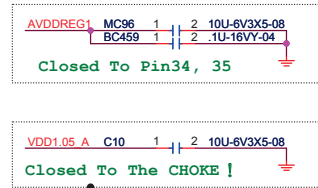
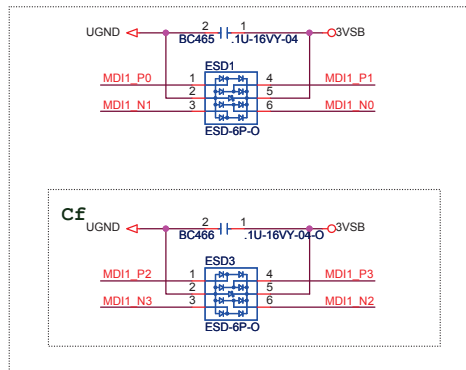
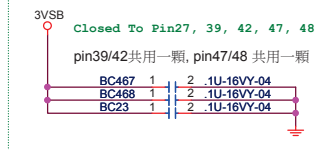
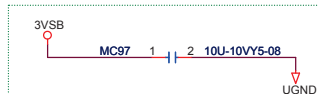
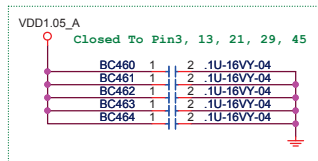
BC16 1 2 .1U-16VY-04
BC17 1 2 .1U-16VY-04

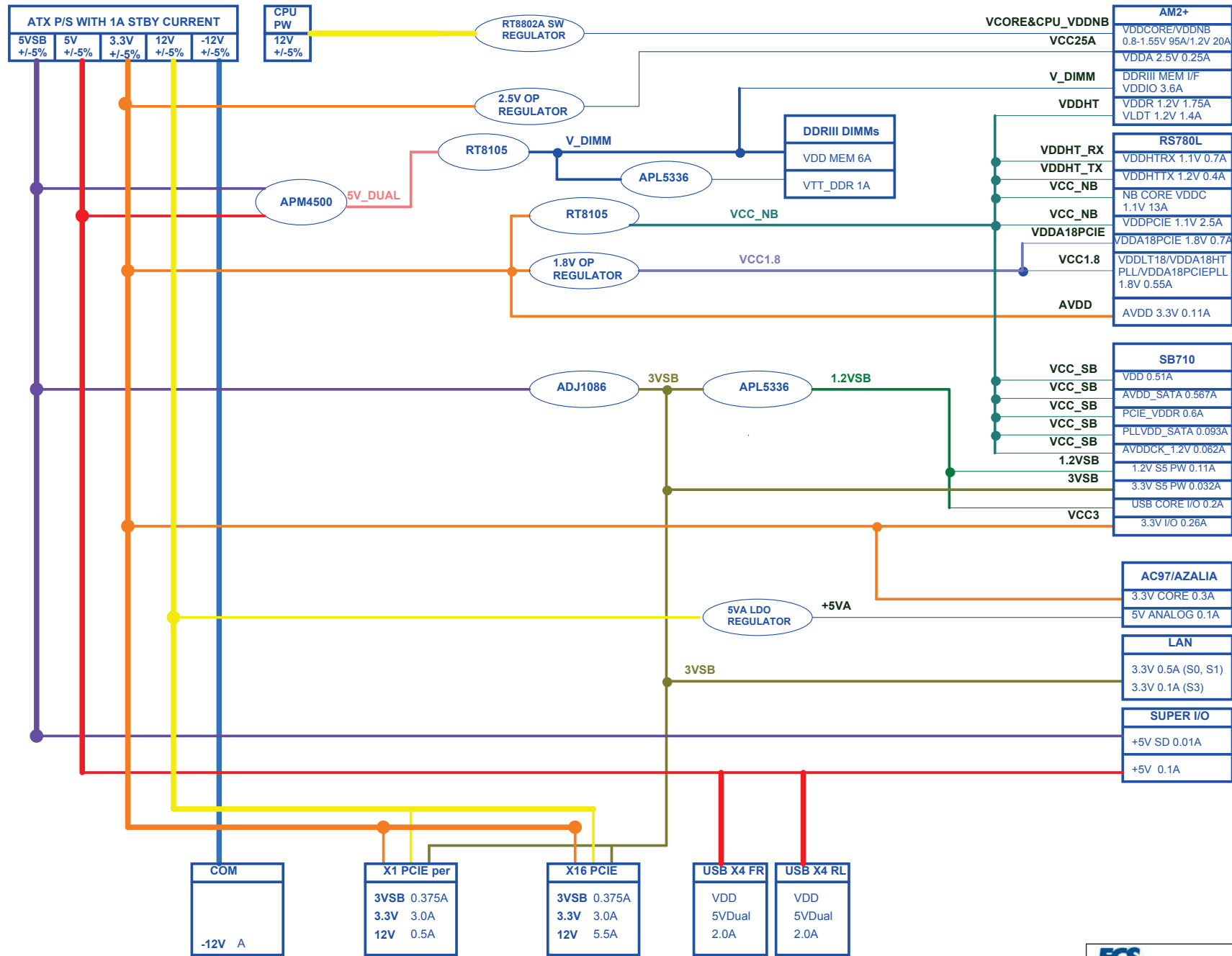
3VSB

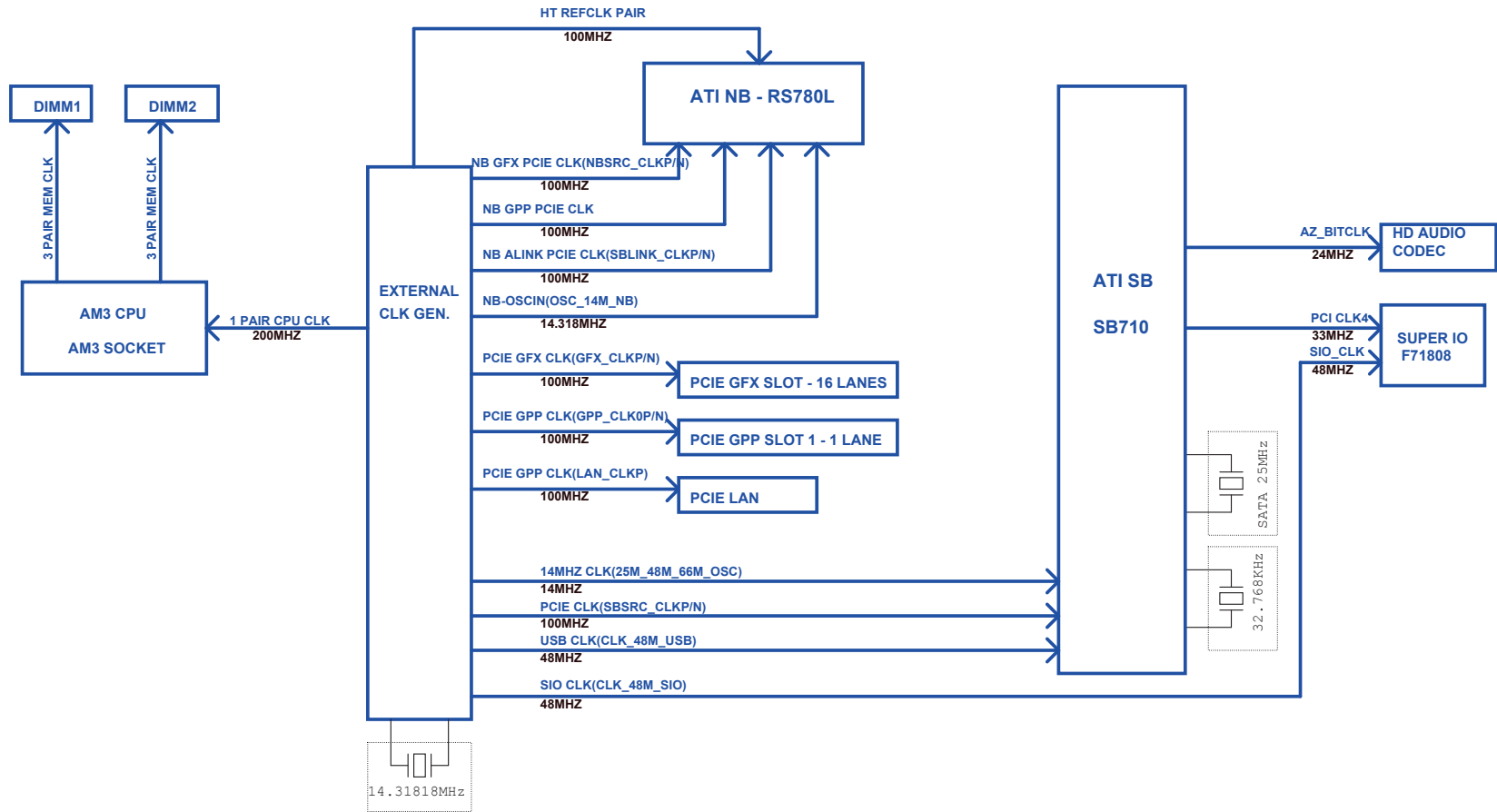
Closed To Pin12

BC15 1 2 .1U-16VY-04

	RTL8111E-VL-CG 100M	RTL8105E-GR 10/100M
Ca	RTL8111E-VL-CG	RTL8105E-VL-CG
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-04
Cf	V	X

[illegible]





Power Sequence

